Compal Confidential

QIQY2 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATi Whistler XT+DDR3

2011-05-11

REV:1.0

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Issued Date	2010/11/30	Deciphered Date	2011/08

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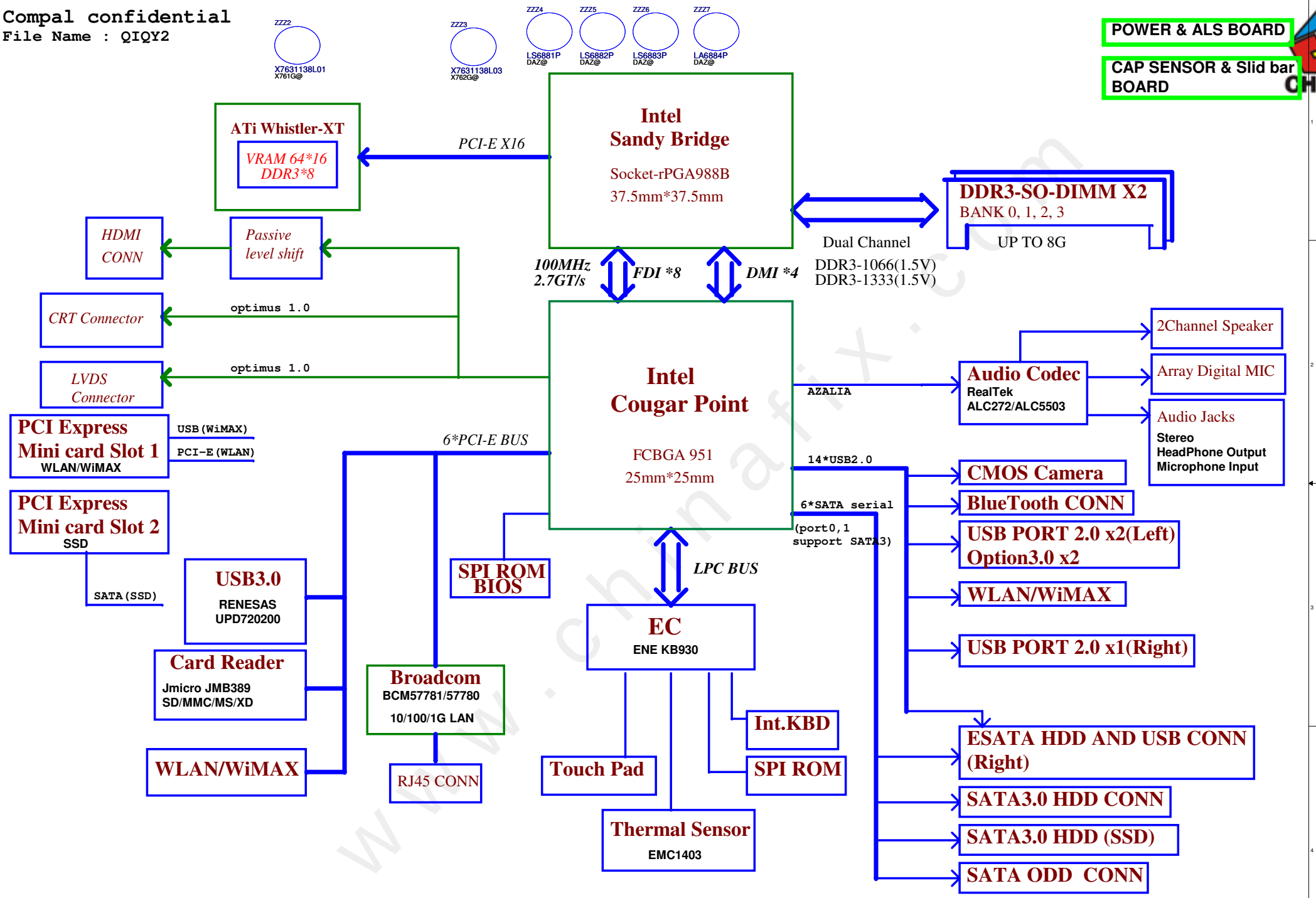

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Title: MB Block Diagram

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	
Camera	CMOS@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

VRAM BOM Config

X761G@ :	X7625738L01	Samsung 1GB
Sub :	X7625738L02	Hynix 1GB
X762G@ :	X7625738L03	Samsung 2GB
Sub :	X7625738L04	Hynix 2GB

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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Power-Up/Down Sequence

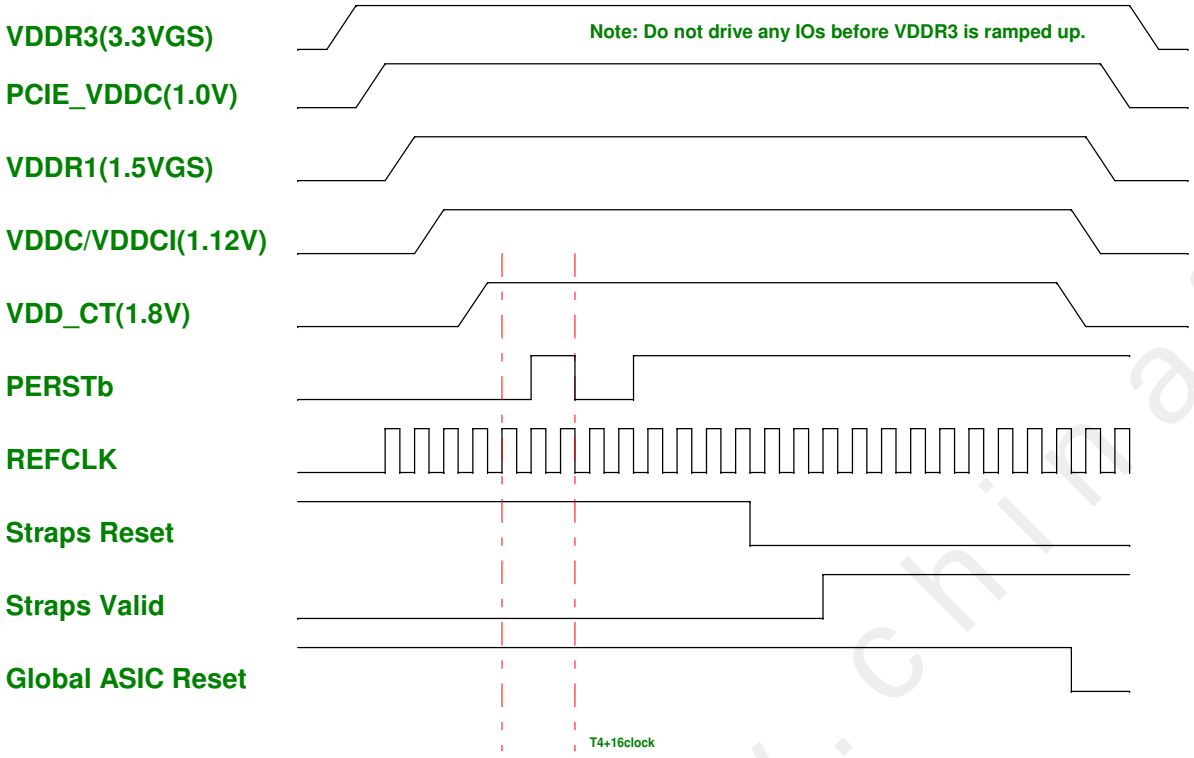
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



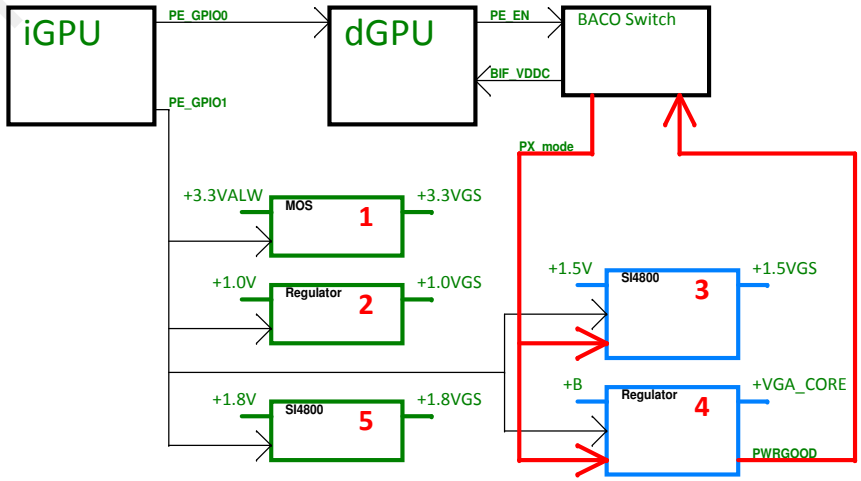
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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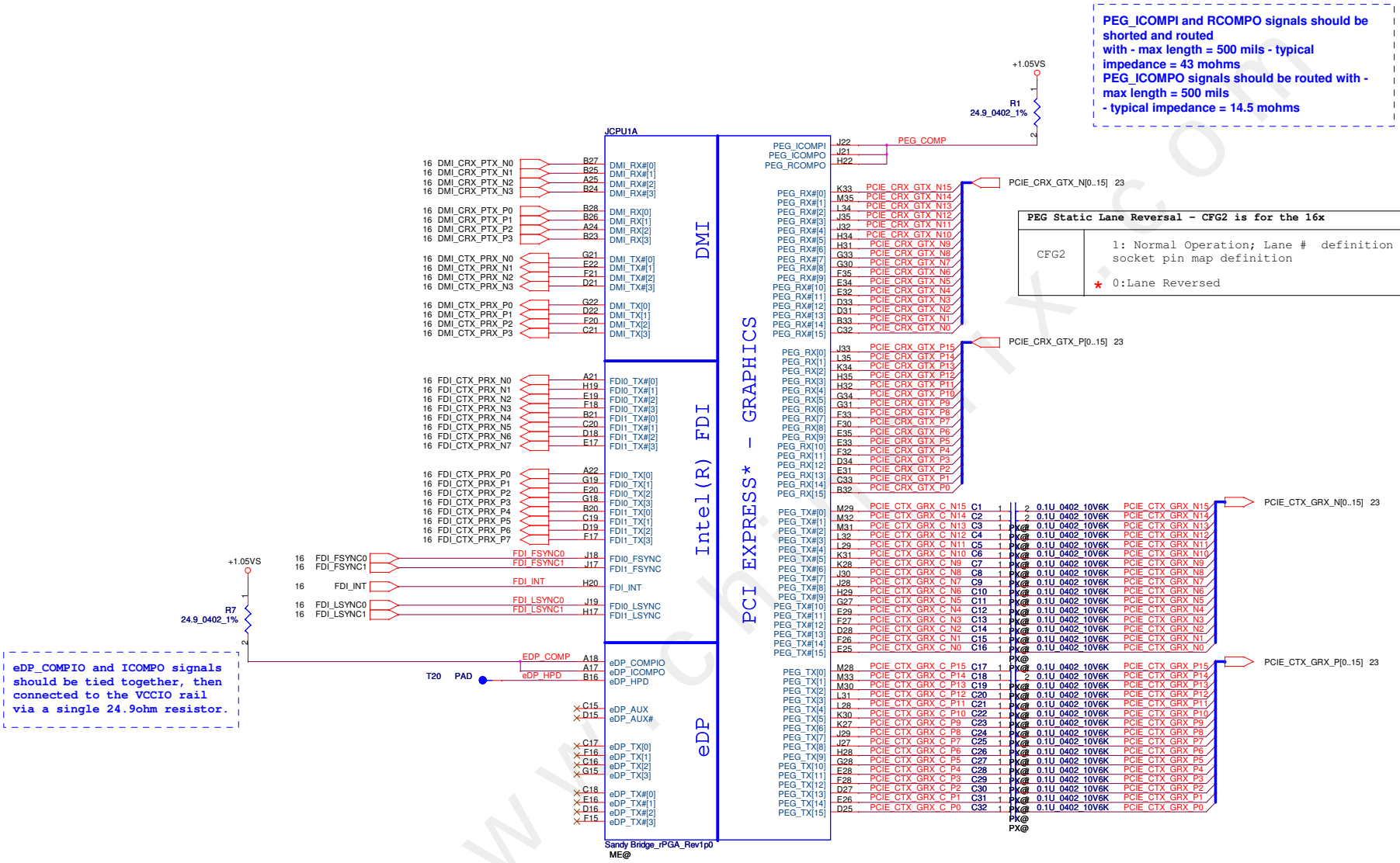

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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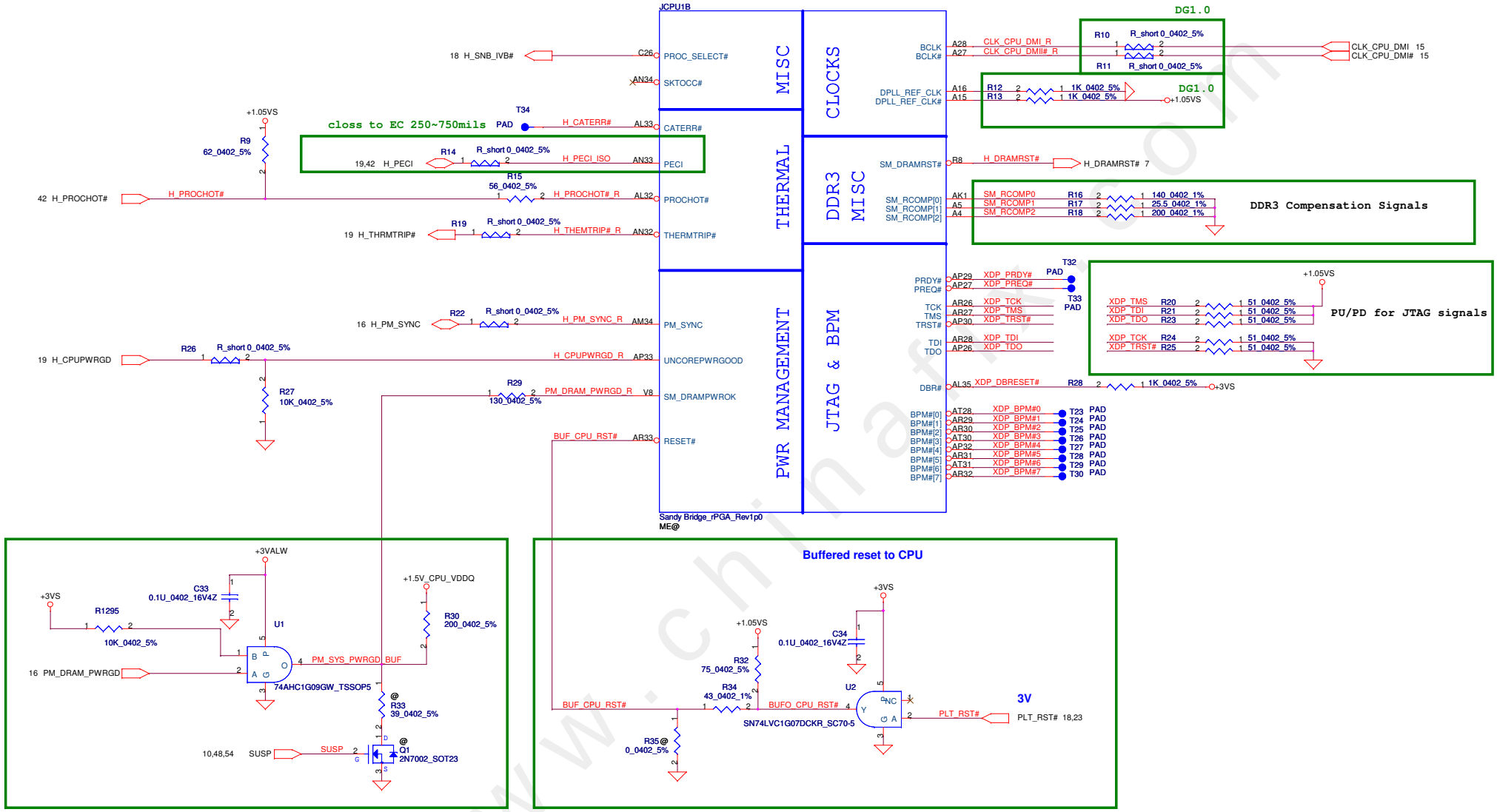

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Title: PROCESSOR(2/7) PM,XDP,CLK

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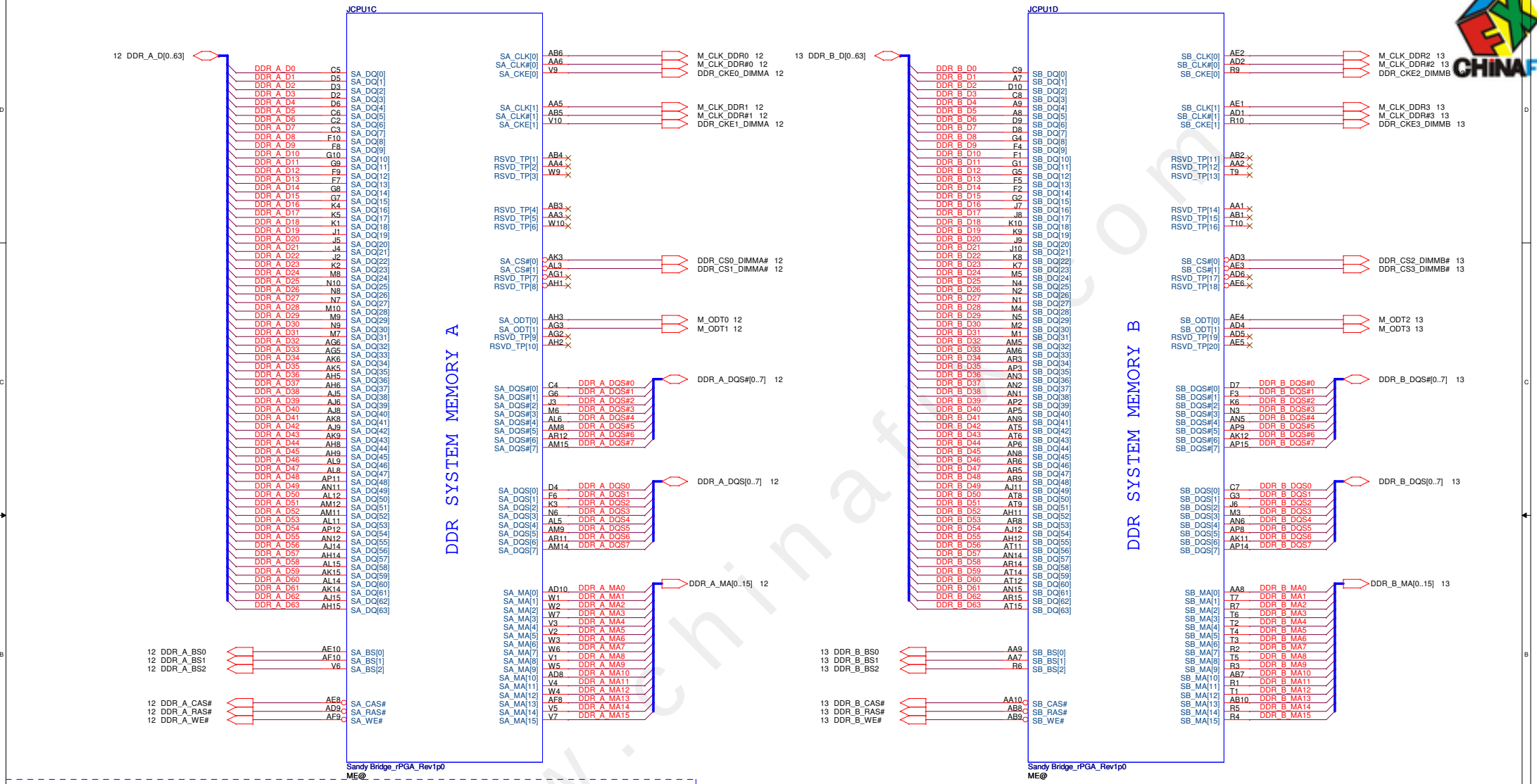

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Title: PROCESSOR(3/7) DDRIII

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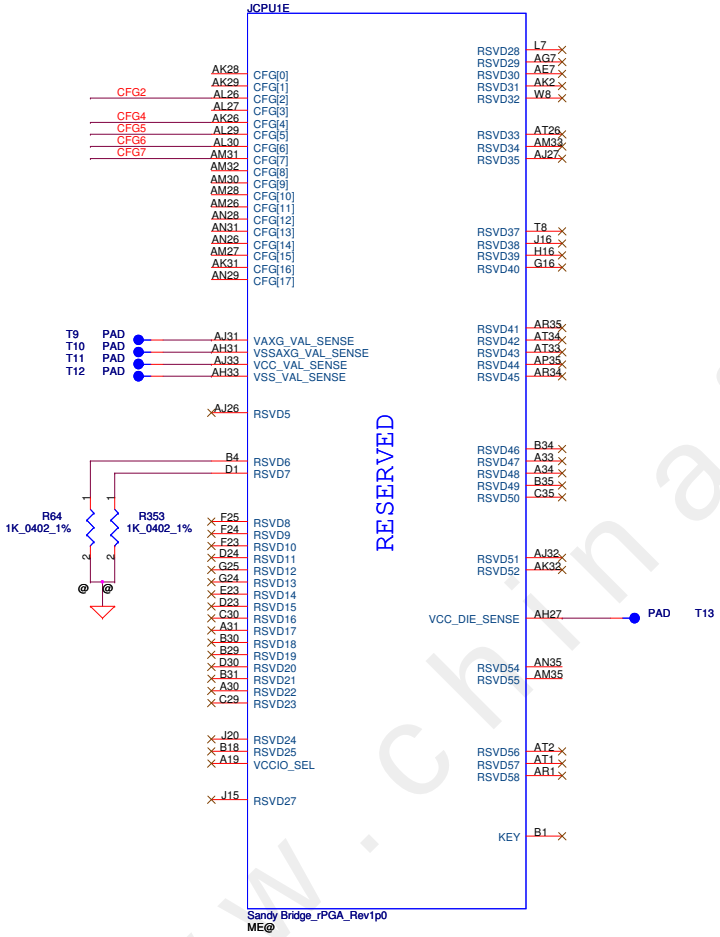
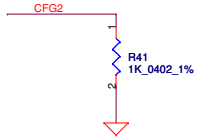
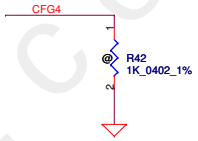
CFG Straps for Processor

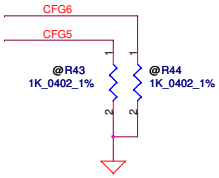




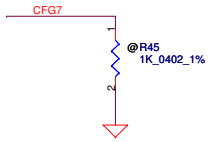
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	★11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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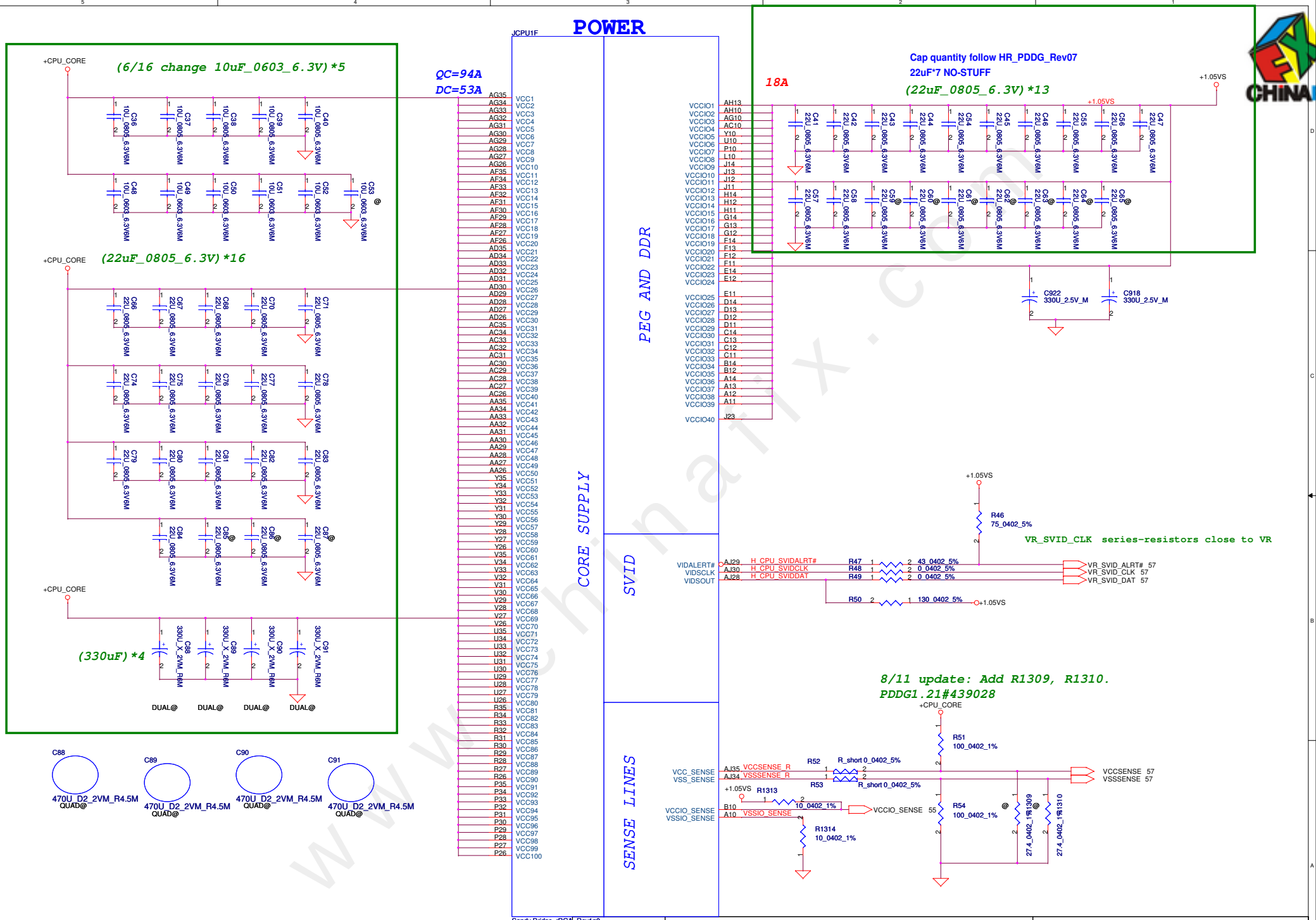

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Title: PROCESSOR(5/7) PWR,BYPASS

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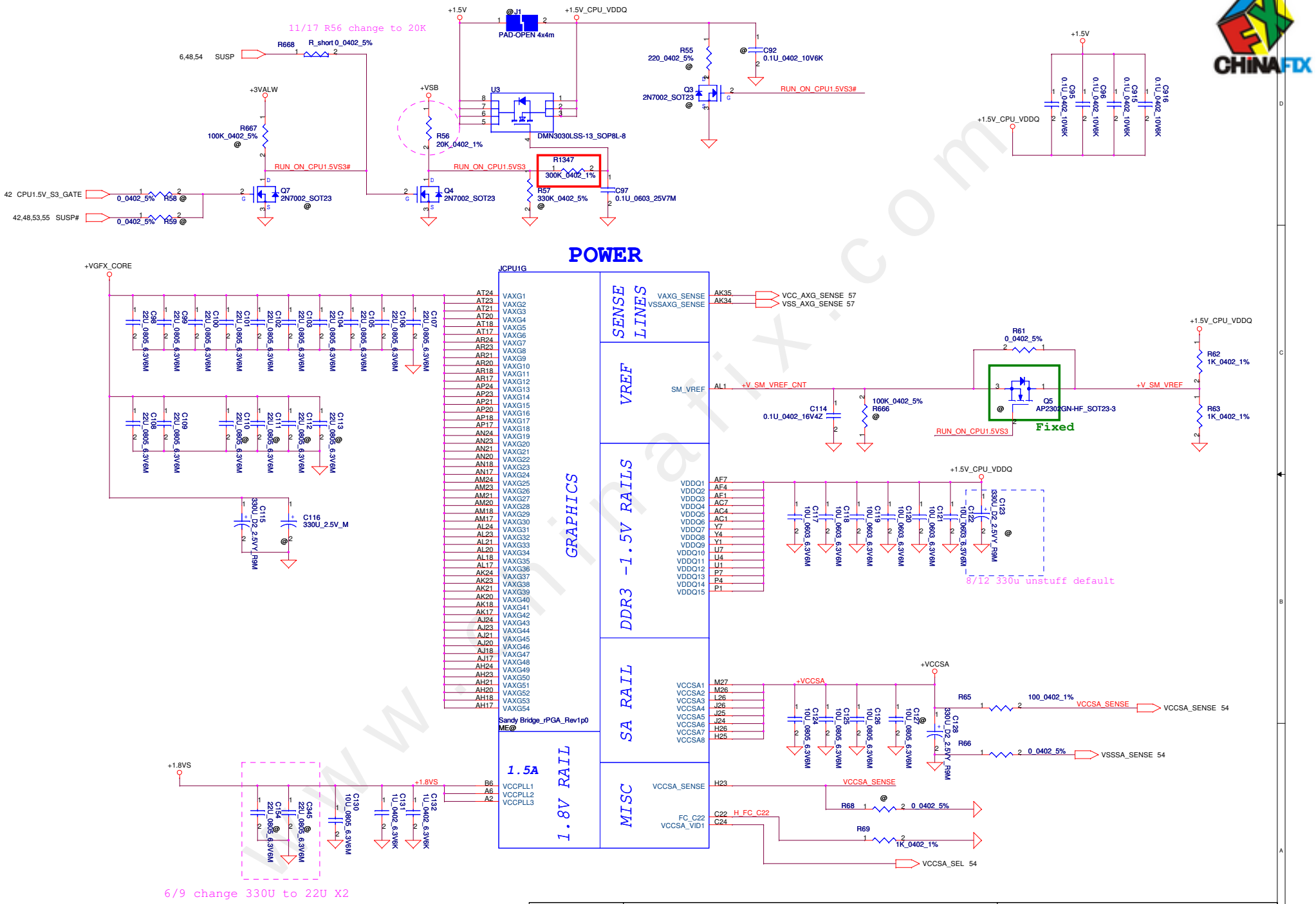

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Title: **PROCESSOR(6/7) PWR**

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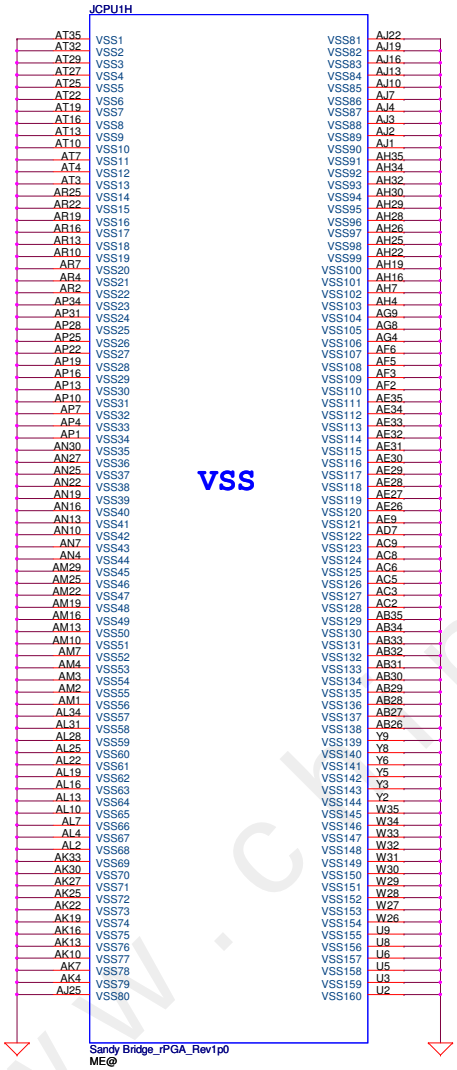

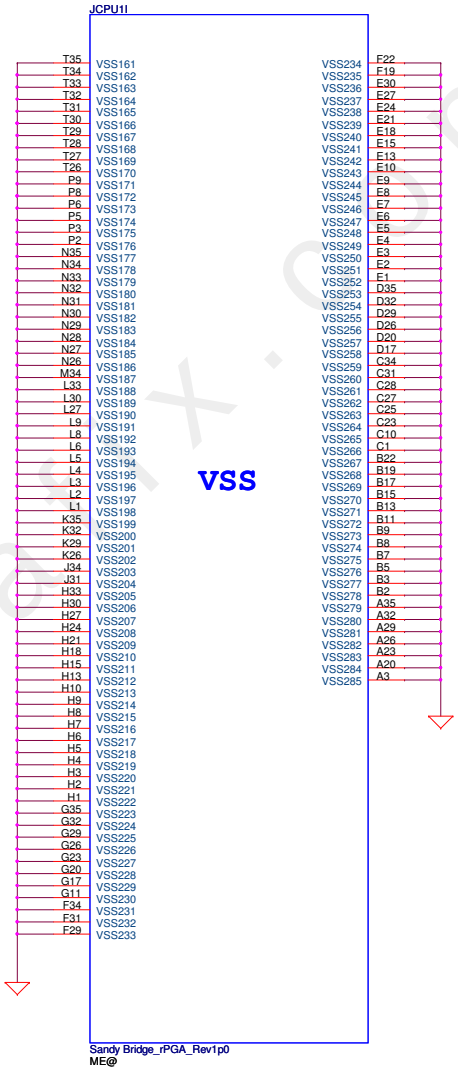

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Title: PROCESSOR(7/7) VSS

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DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4526-0100

ME@

7 DDR_A_D[0..63]
7 DDR_A_DQS[0..7]
7 DDR_A_DQS#[0..7]
7 DDR_A_MA[0..15]

R70 1K_0402_1% +VREF_DQ_DIMMA
R71 1K_0402_1%

C133 0.1U_0402_10V6K
C134 2.2U_0603_6.3V6K

R72 1K_0402_1%
R73 1K_0402_1%
C135 0.1U_0402_10V6K
C136 2.2U_0603_6.3V6K

R81 10K_0402_5%
C155 2.2U_0603_6.3V6K
C156 0.1U_0402_10V6K
R83 10K_0402_5%

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)
VTT(0.75V) =
3*0805 10uf 4*0402 1uf
VREF =
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

C137 10U_0603_6.3V6M @
C138 10U_0603_6.3V6M @
C139 10U_0603_6.3V6M
C140 10U_0603_6.3V6M
C141 10U_0603_6.3V6M
C142 10U_0603_6.3V6M
C143 10U_0603_6.3V6M
C144 10U_0603_6.3V6M
C145 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 220U_B2_2.5VM_R35

Layout Note:
Place near DIMM

C150 C151 C152 C153 1U_0402_6.3V6K

Layout Note:
Short to ground

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Title: DDRIII-SODIMM SLOT1

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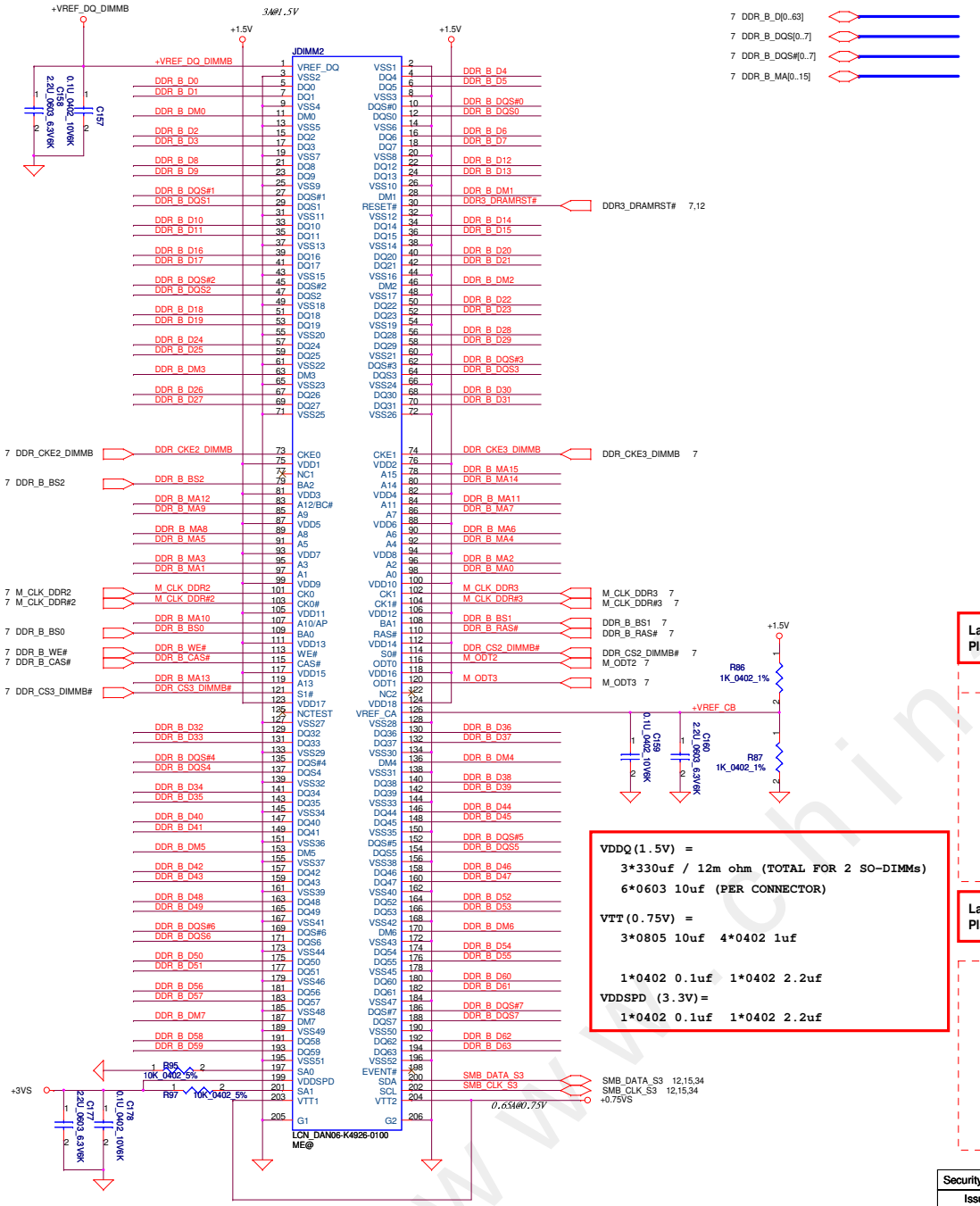
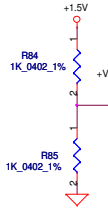




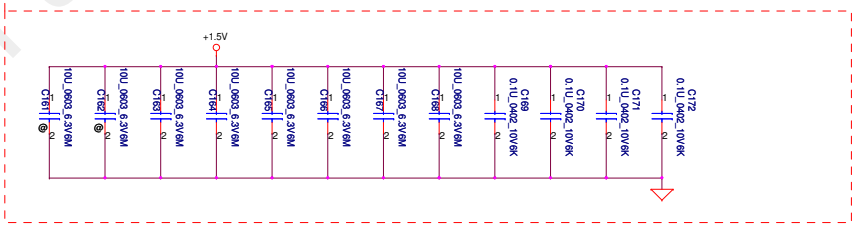
For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

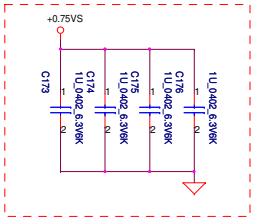
Layout Note:
Place near DIMM

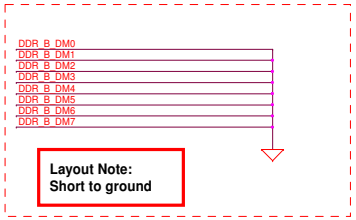
(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4



Layout Note:
Place near DIMM





Layout Note:
Short to ground

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size | Document Number: QIQY2 LA6884P | Rev 1.0

Date: Wednesday, May 11, 2011 | Sheet 13 of 60

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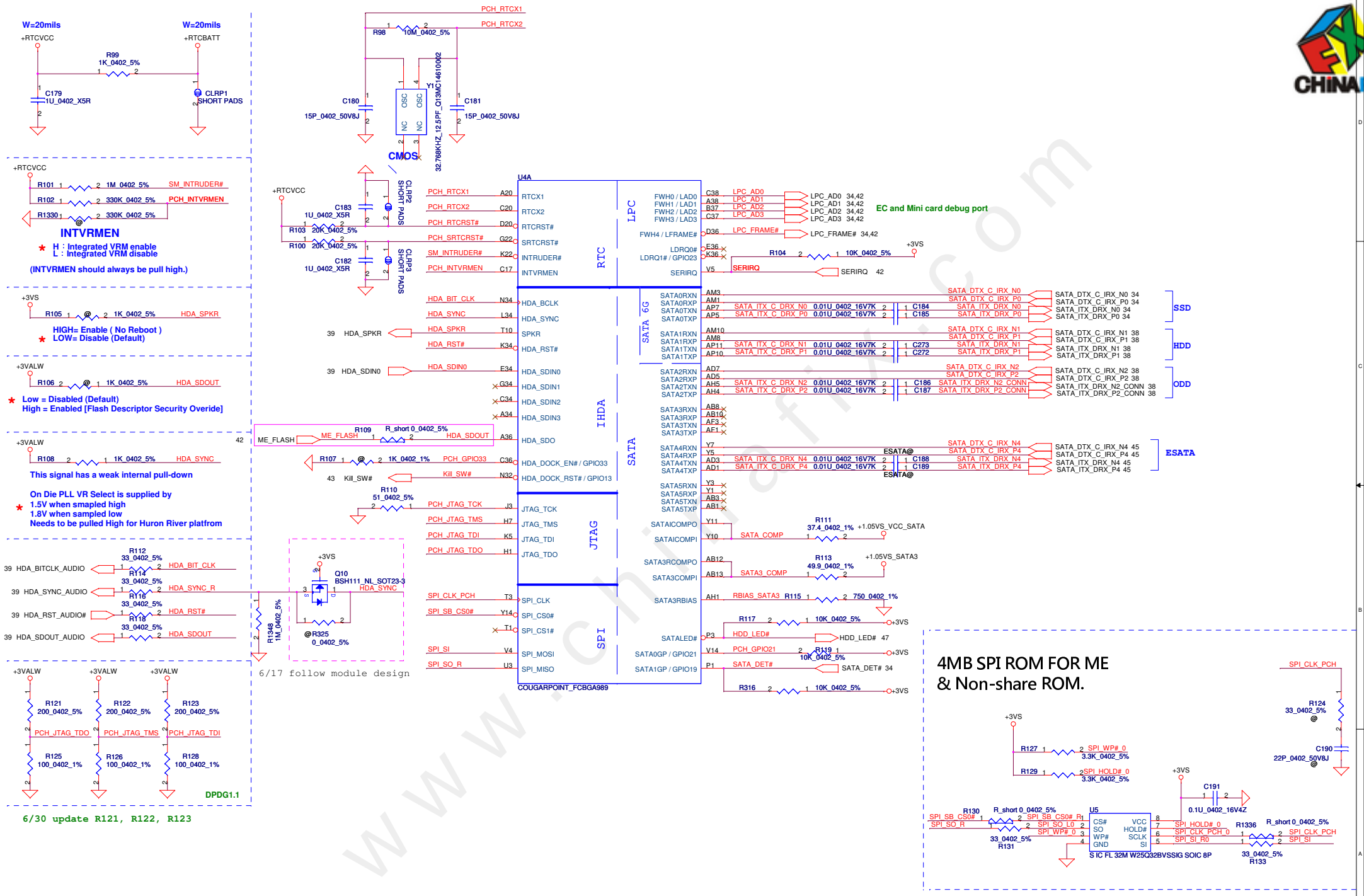

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Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

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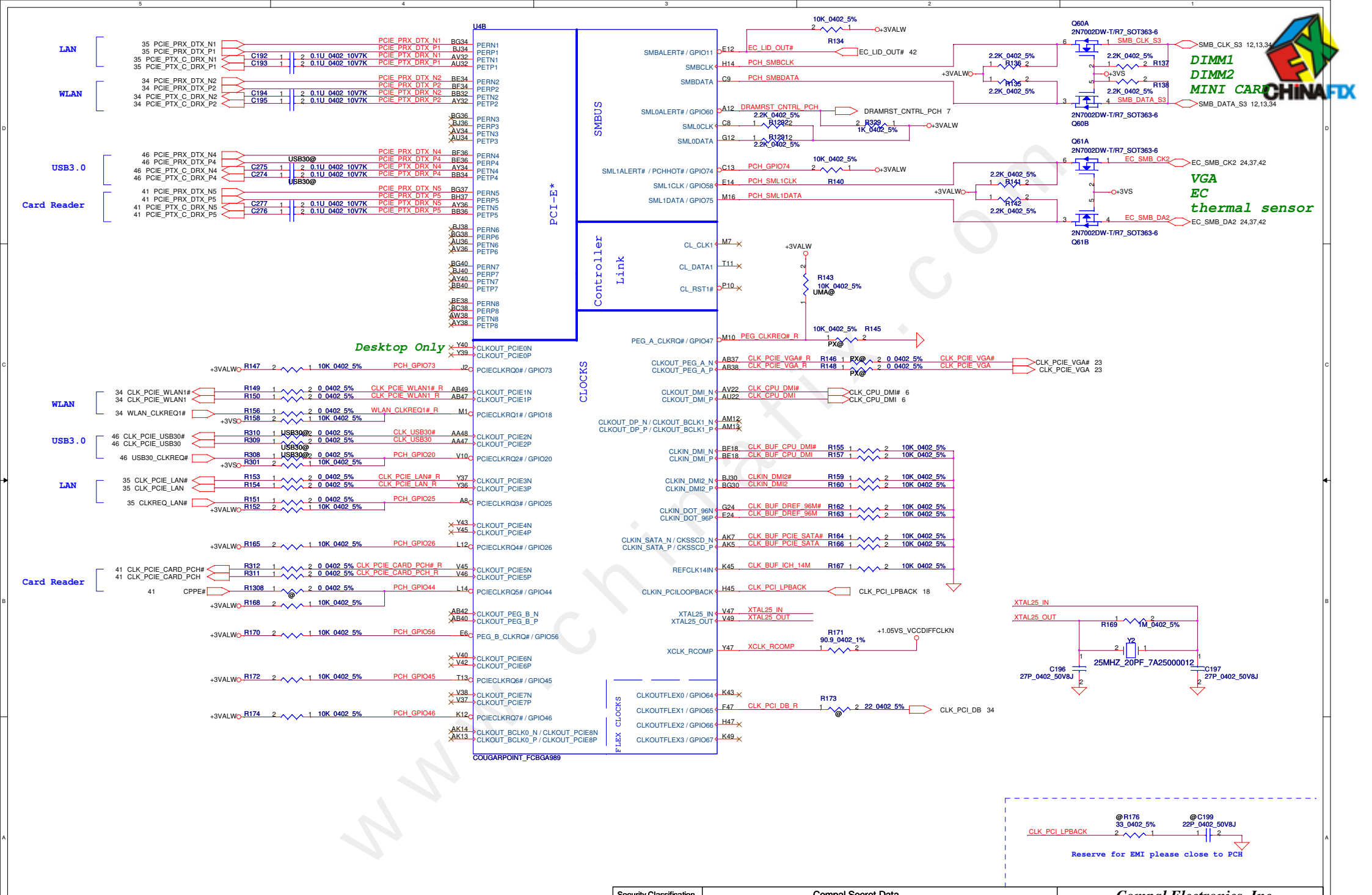

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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 15 of 60

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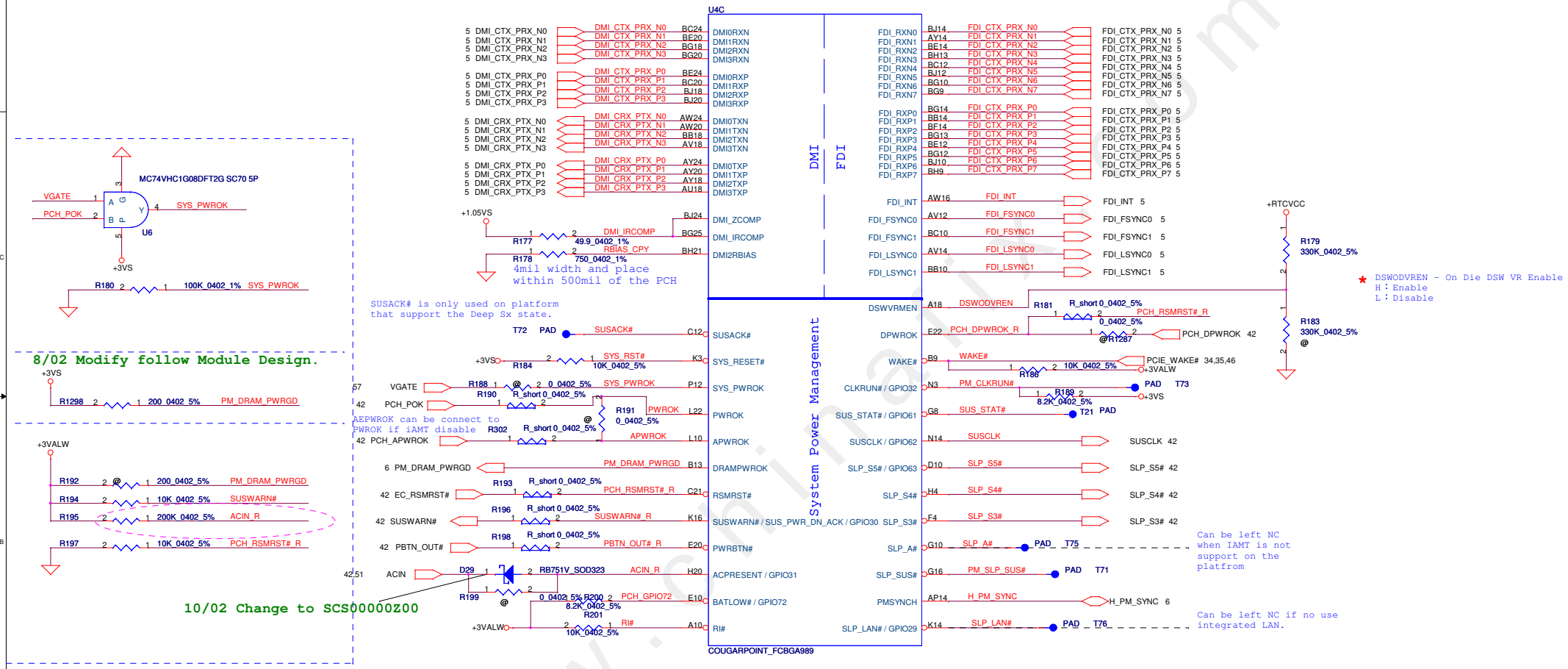

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Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

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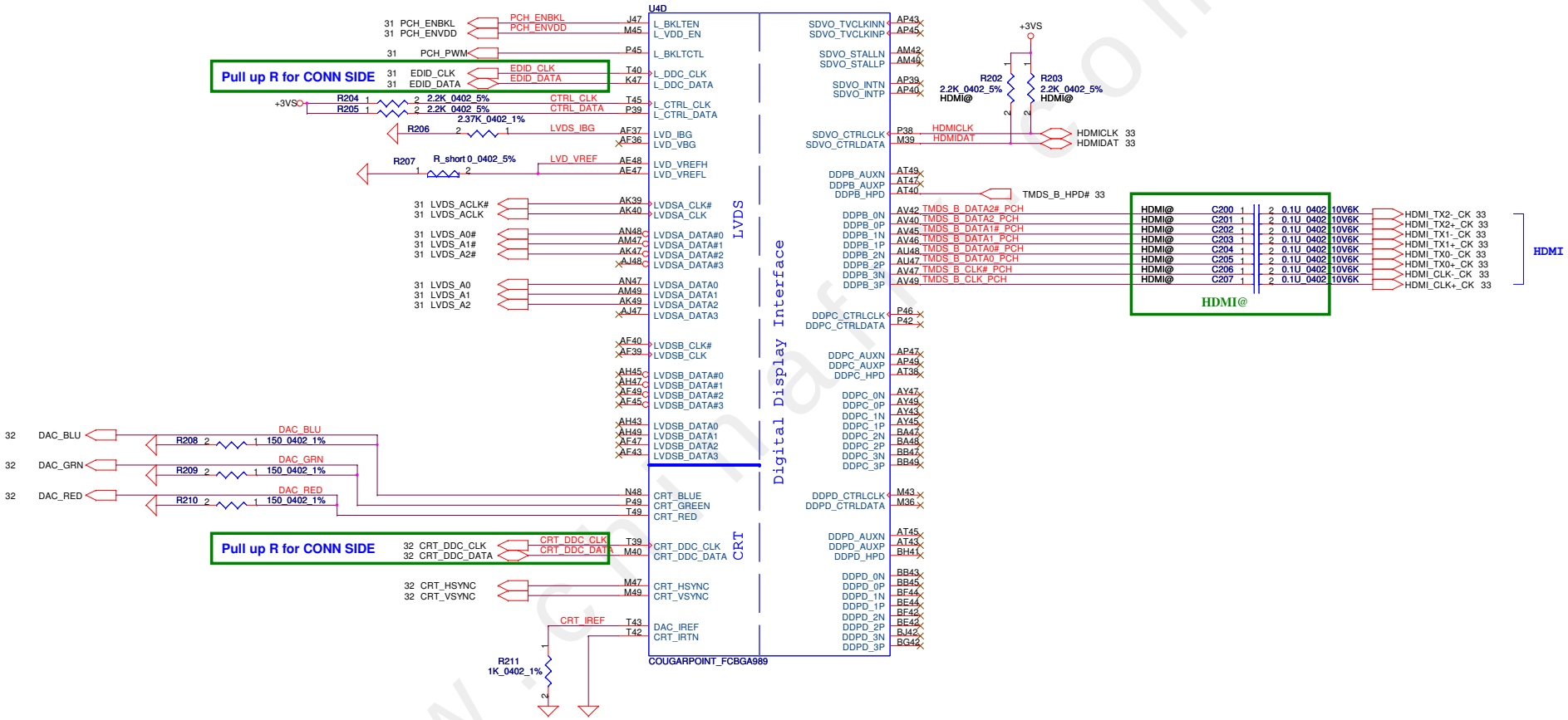

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

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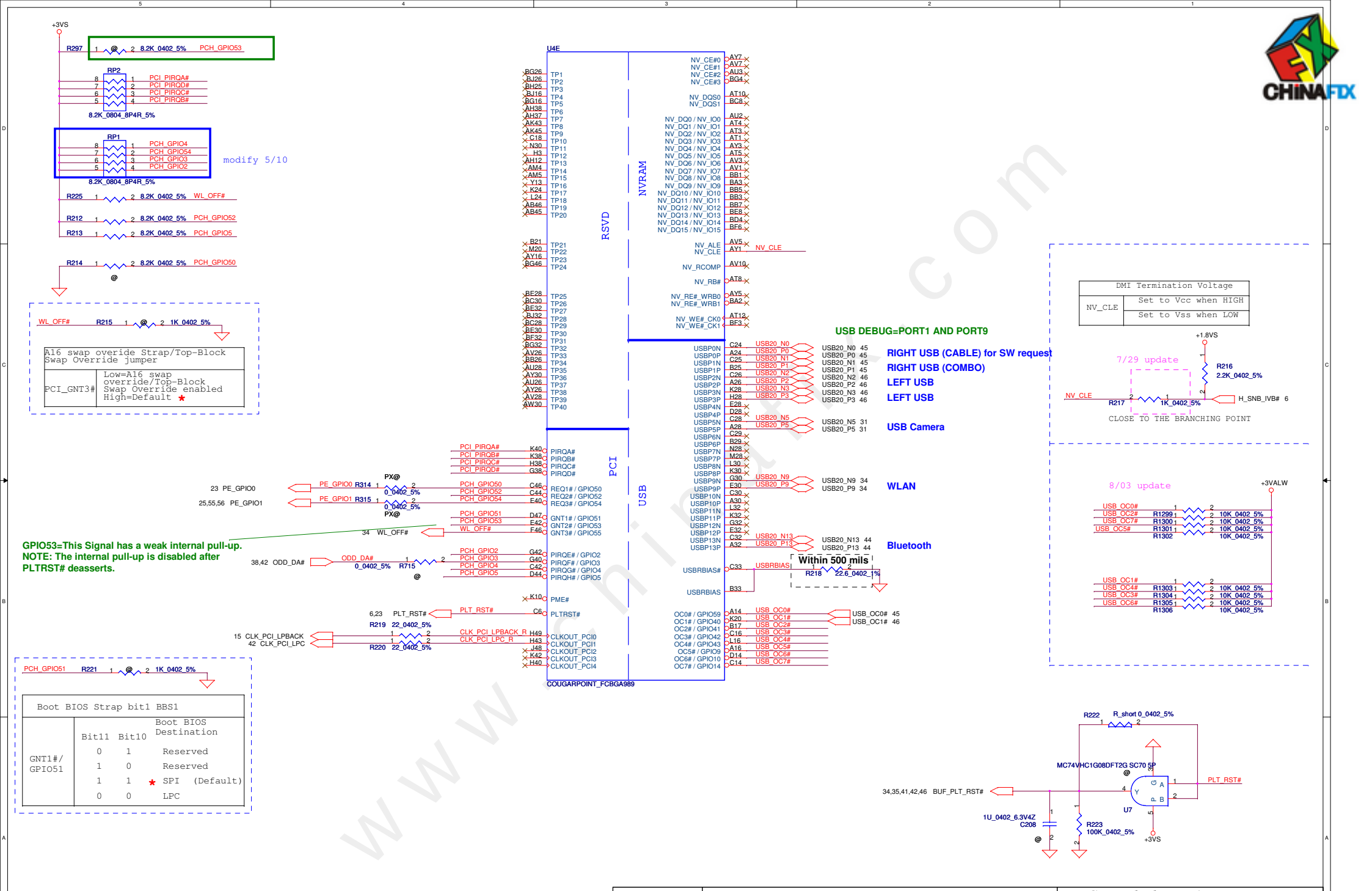

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

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Date: Wednesday, May 11, 2011 | Sheet 18 of 60

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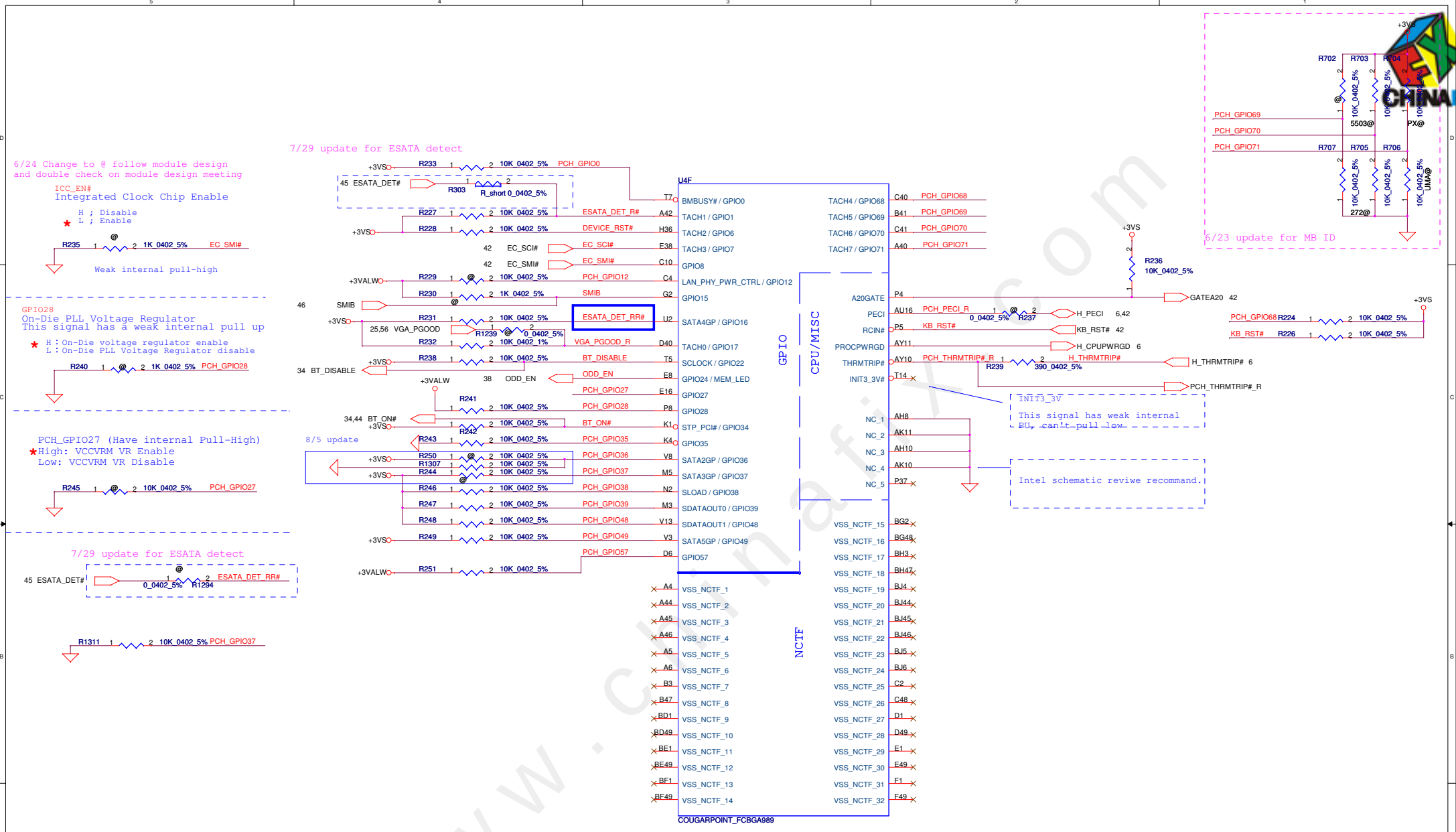

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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Date: Wednesday, May 11, 2011 | Sheet 19 of 60

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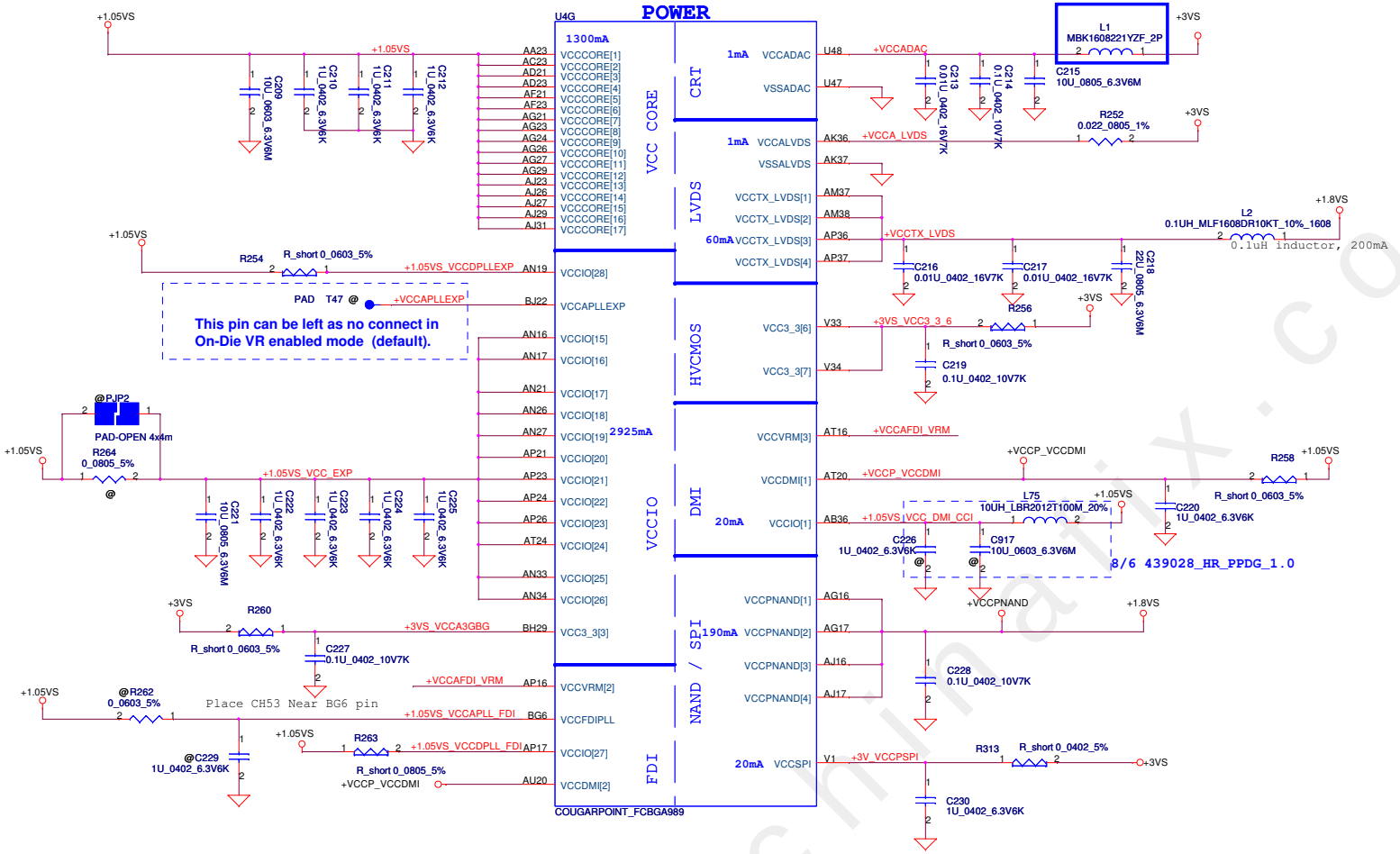
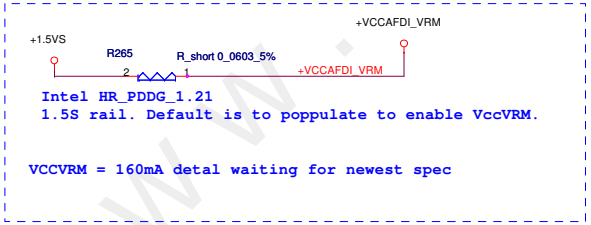
modify 5/02 from bead SM01000AX00
change to 1 ohm SD014100B80





PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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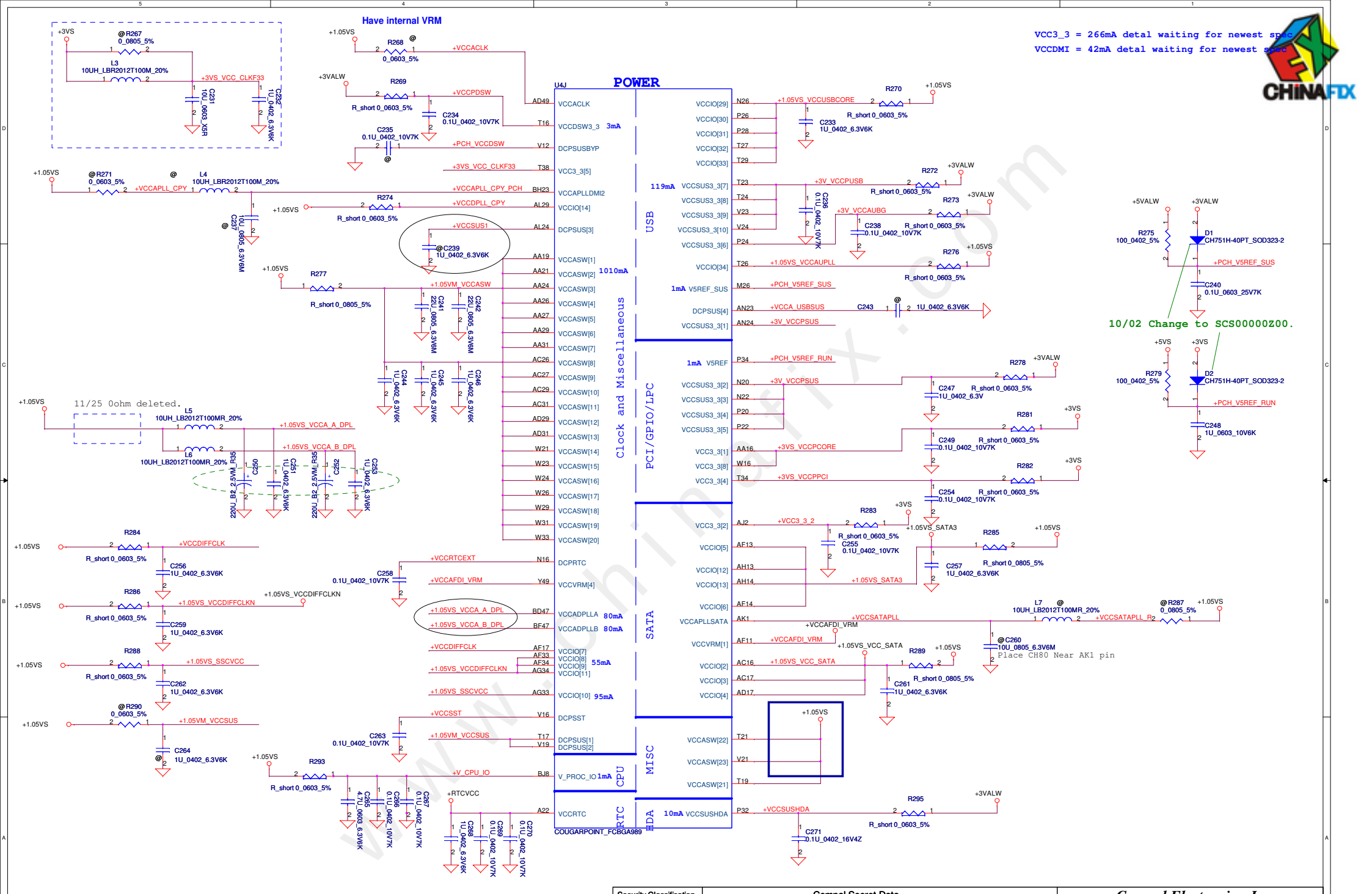
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 20 of 60



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Compal Electronics, Inc.

Title: PCH (8/9) PWR

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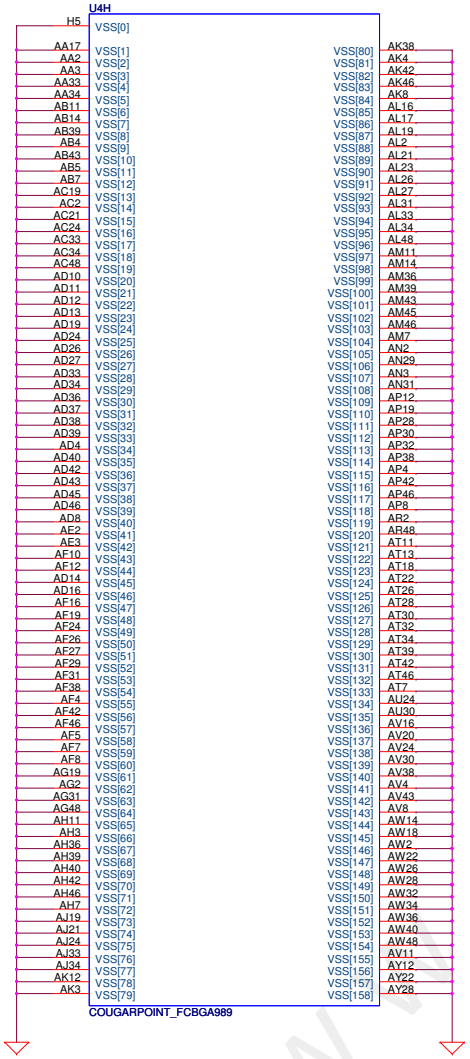

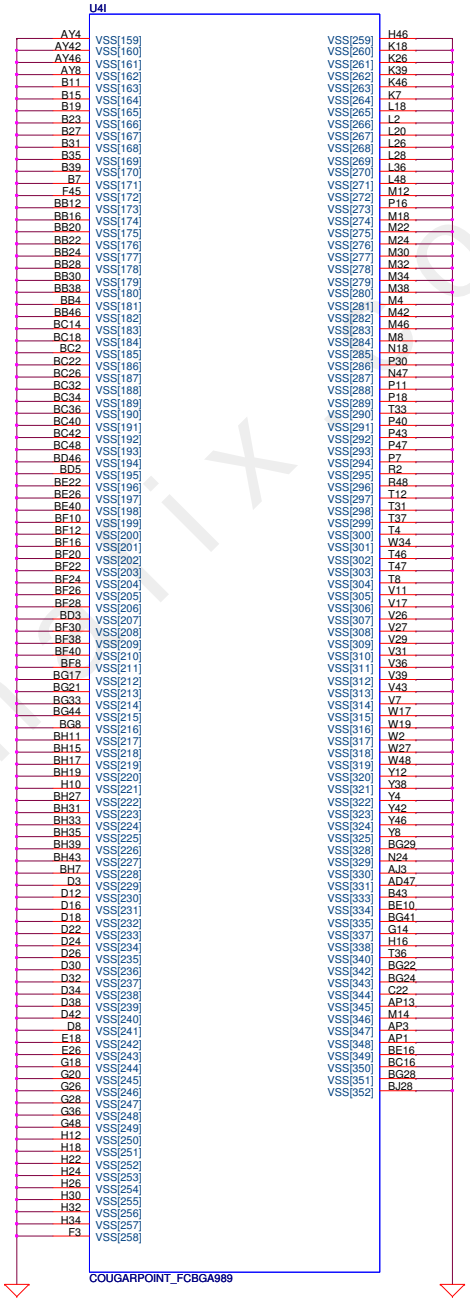

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Compal Electronics, Inc.

Title: PCH (9/9) VSS

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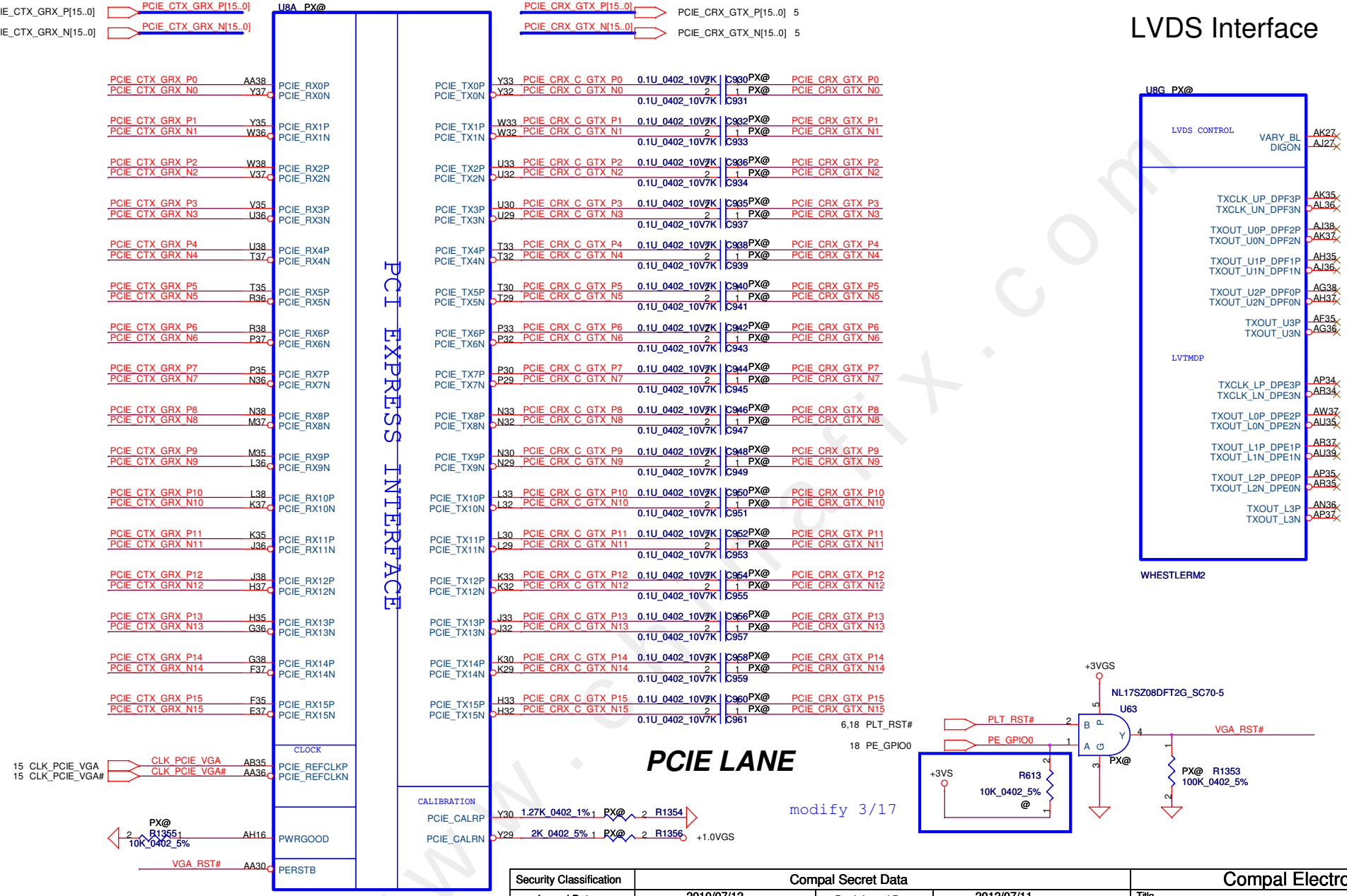
LVDS Interface



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Compal Electronics, Inc.

Title: ATI_Whistler_M2_PEG & LVDS

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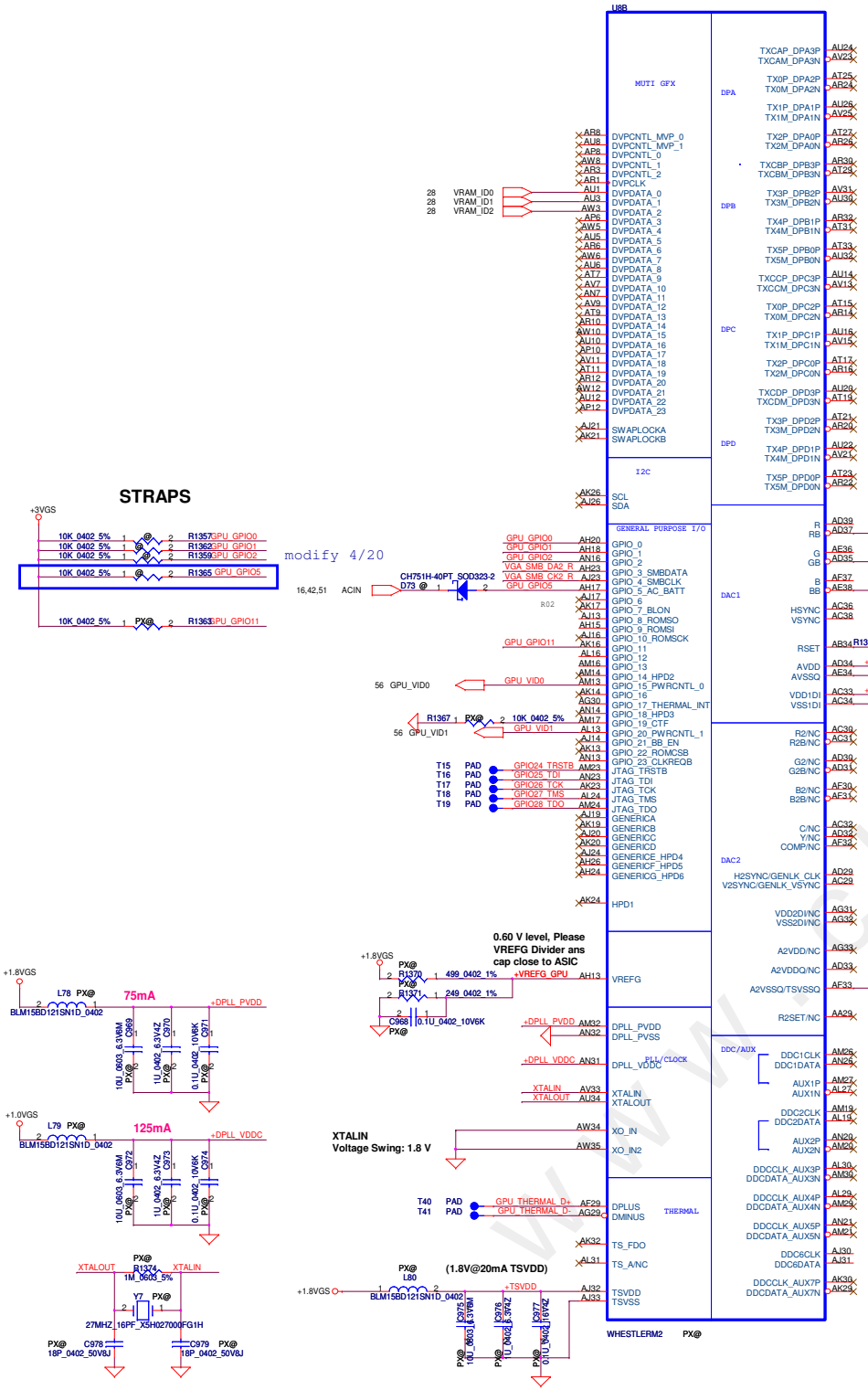


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

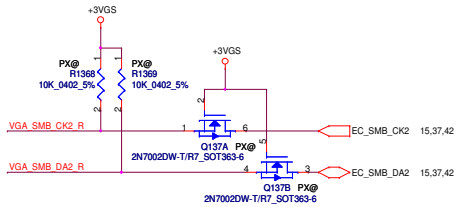
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Internal VGA Thermal Sensor



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Compal Electronics, Inc.

Title: ATI_Whistler_M2_Main\MSIC

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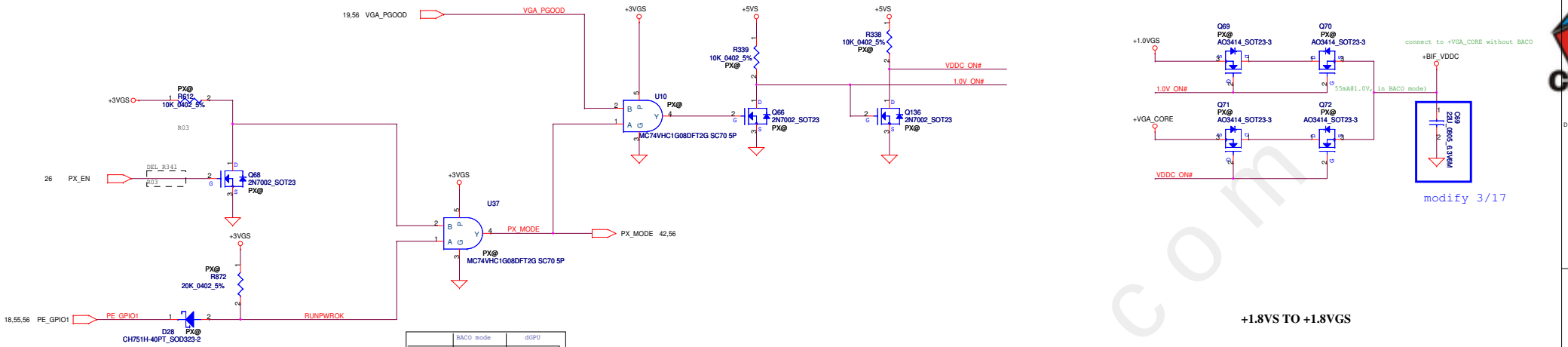
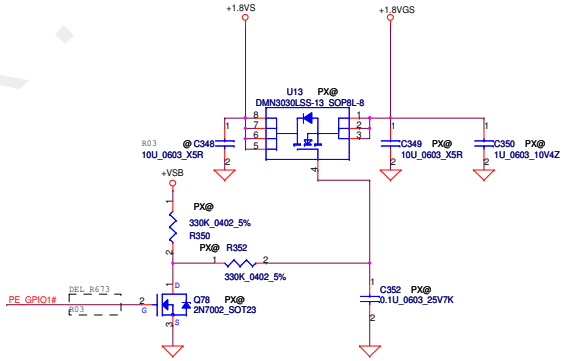


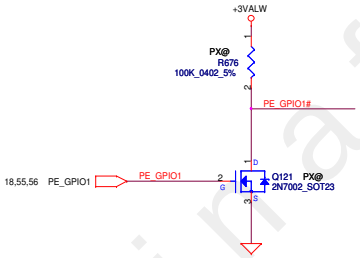
D28 with leakage need to check

	BACO mode	dGPU
PX_EN	1	0
PE_GPIO1	0	1
PX_MODE	0	1
VGA_PGOOD	0	1
VDDC_ON#	0	1
1.0V_ON#	1	0
+BIF_VDDC	+1.0VGS	VGA_CORE

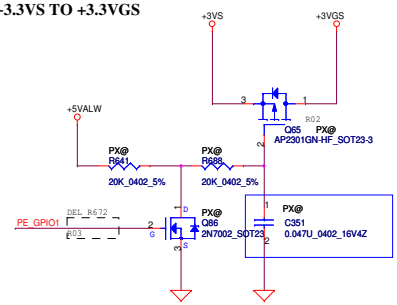
modify 3/17

+1.8VS TO +1.8VGS



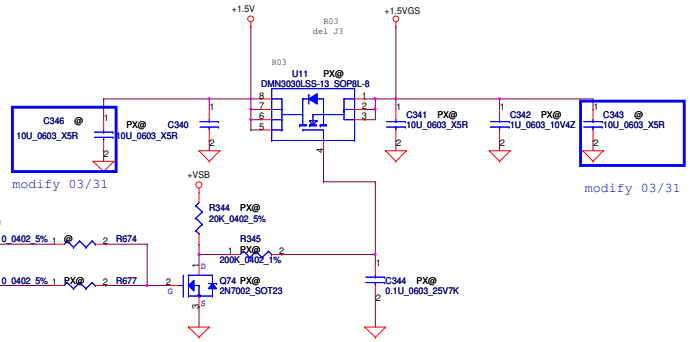


+3.3VS TO +3.3VGS



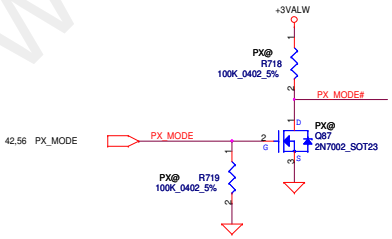
modify 03/25

+1.5VS TO +1.5VGS



modify 03/31

modify 03/31



PX3.0 use

PE_GPIO1# 0_0402_5% @ R674

PX_MODE# 0_0402_5% PX@ R677

BACO use

Q74 PX@
2N7002_SOT23

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Title: ATI_Whistler_M2_BACO

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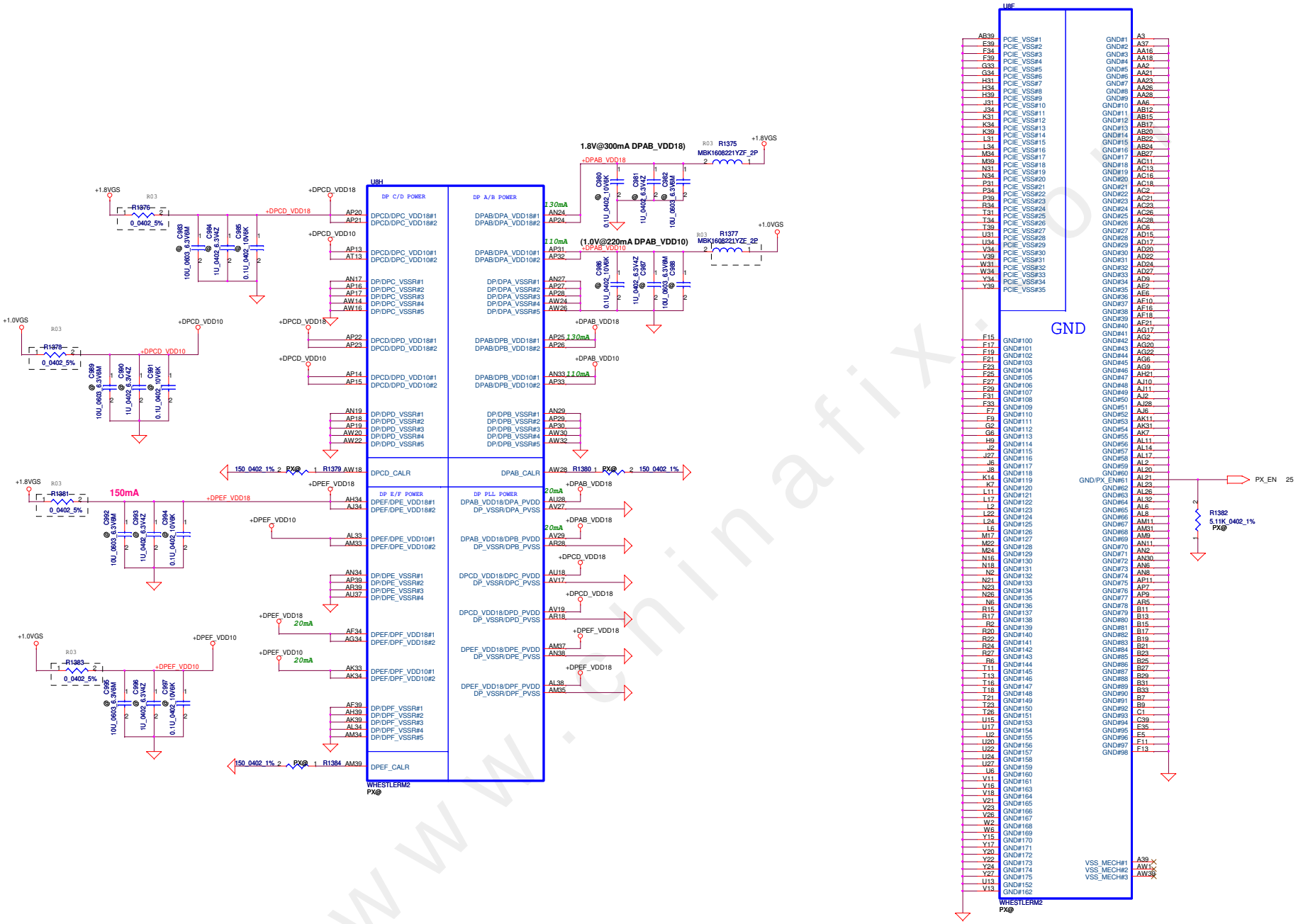

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_DPX PWR_GND

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Date: Wednesday, May 11, 2011 | Sheet 26 of 60

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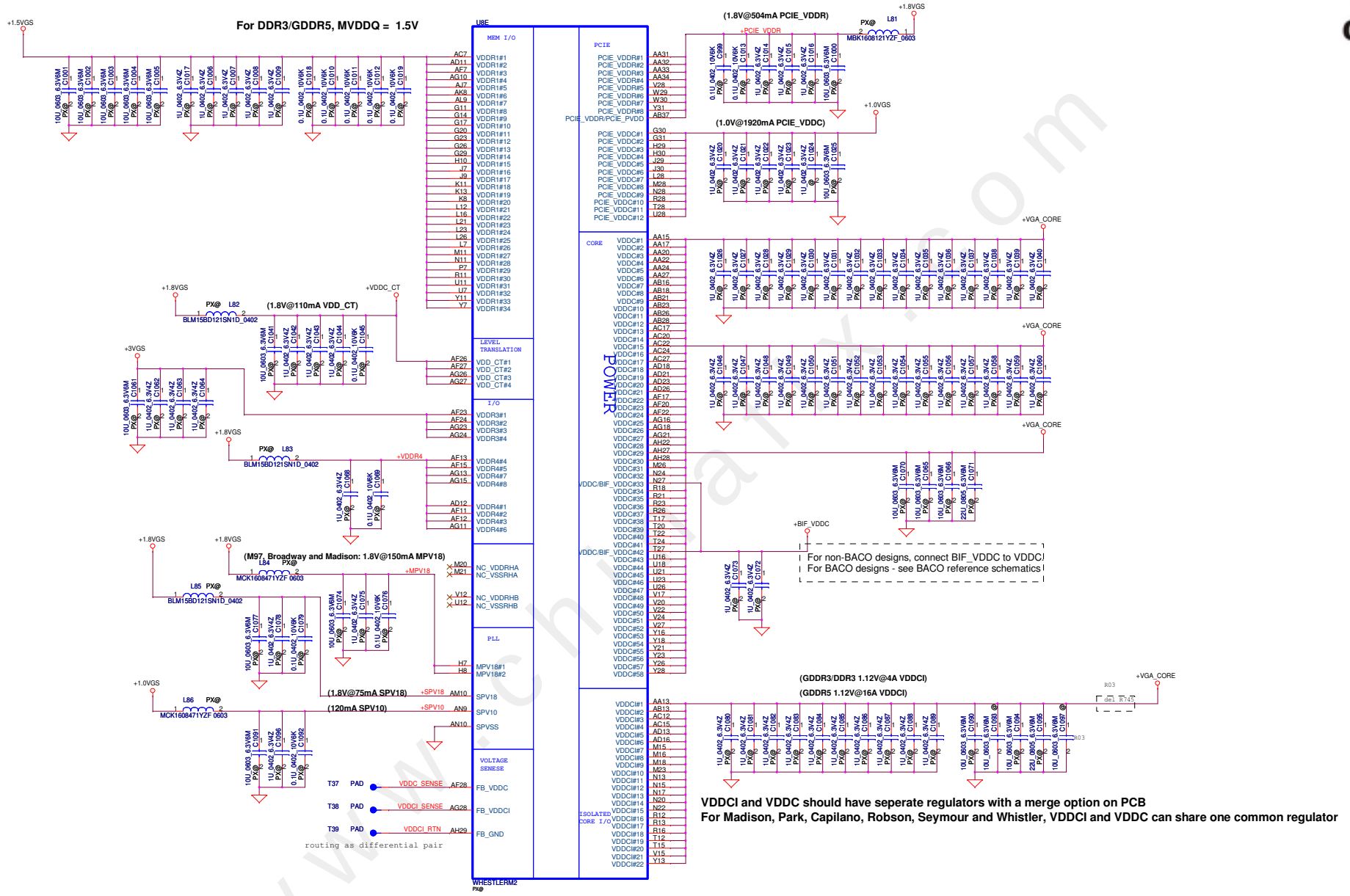

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_Power

Size: C | Document Number | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 27 of 60

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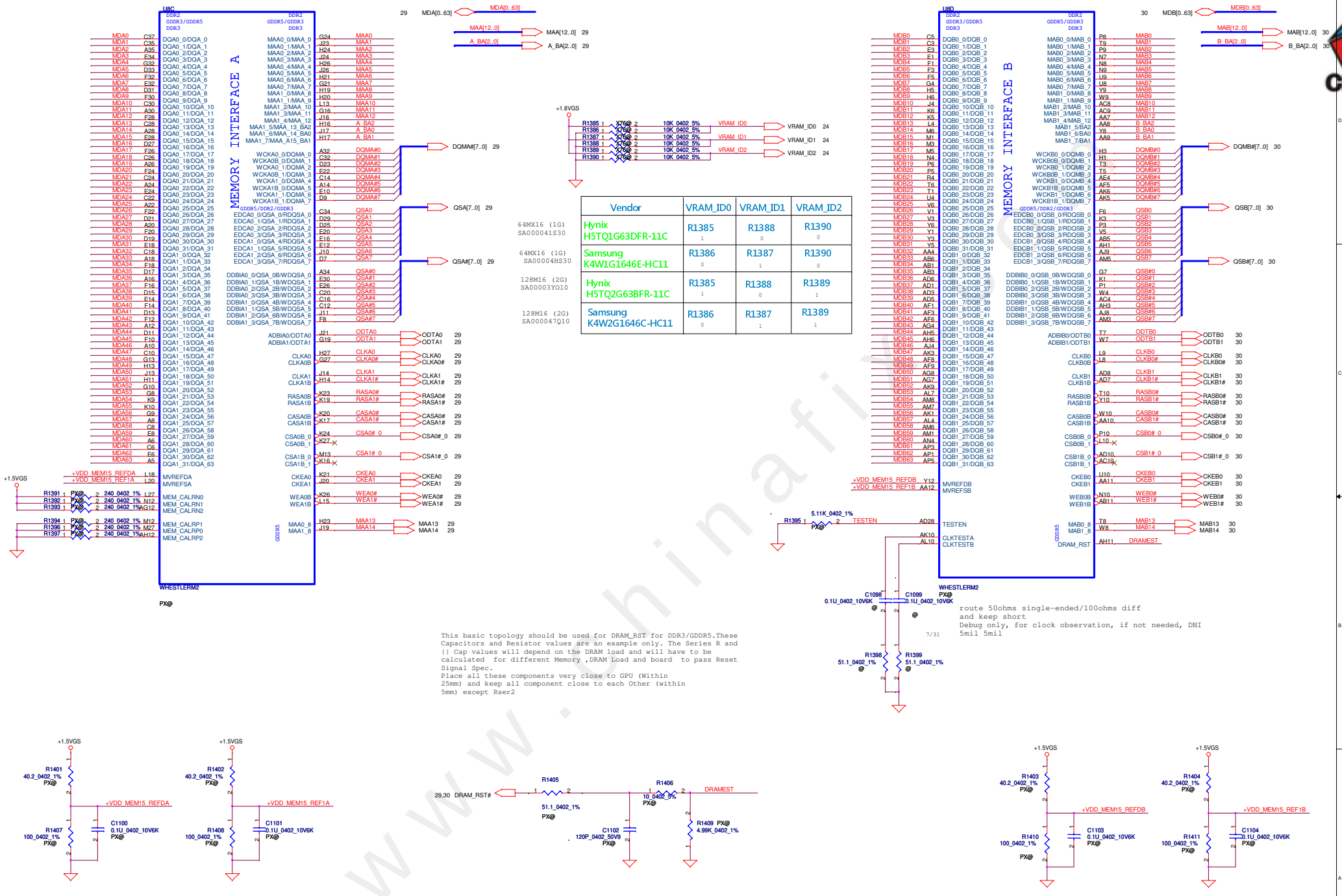

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63DFR-11C	R1385 1	R1388 0	R1390 0
Samsung K4W1G1646E-HC11	R1386 0	R1387 1	R1390 0
Hynix H5TQ2G63BFR-11C	R1385 1	R1388 0	R1389 1
Samsung K4W2G1646C-HC11	R1386 0	R1387 1	R1389 1

64MX16 (1G) SA000041S30
64MX16 (1G) SA00004HS30
128M16 (2G) SA00003YO10
128M16 (2G) SA000047Q10

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_MEM IF

Size: C | Document Number | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 28 of 60

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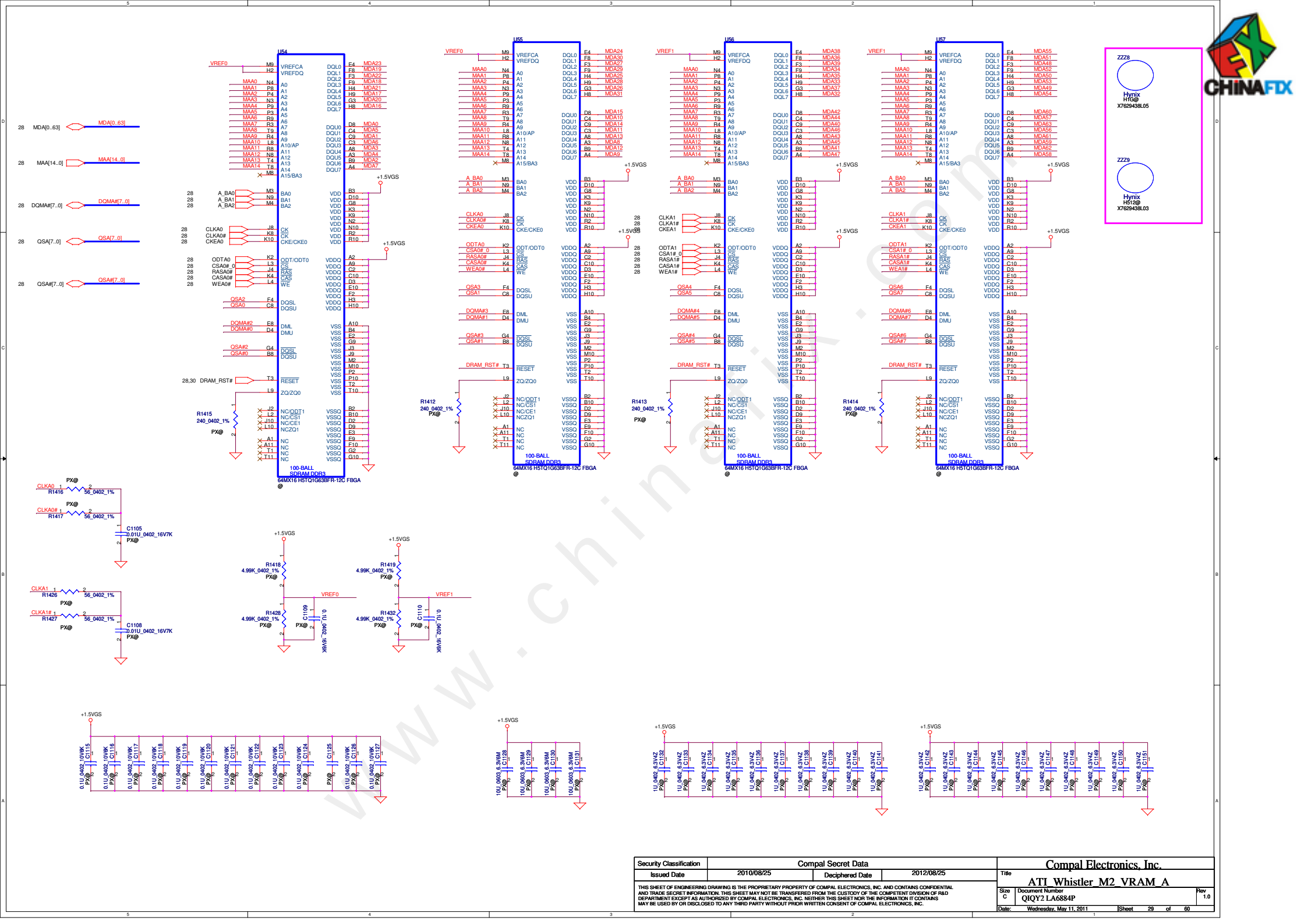

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	QIQY2 LA6884P	1.0

Date: Wednesday, May 11, 2011 | Sheet 29 of 60

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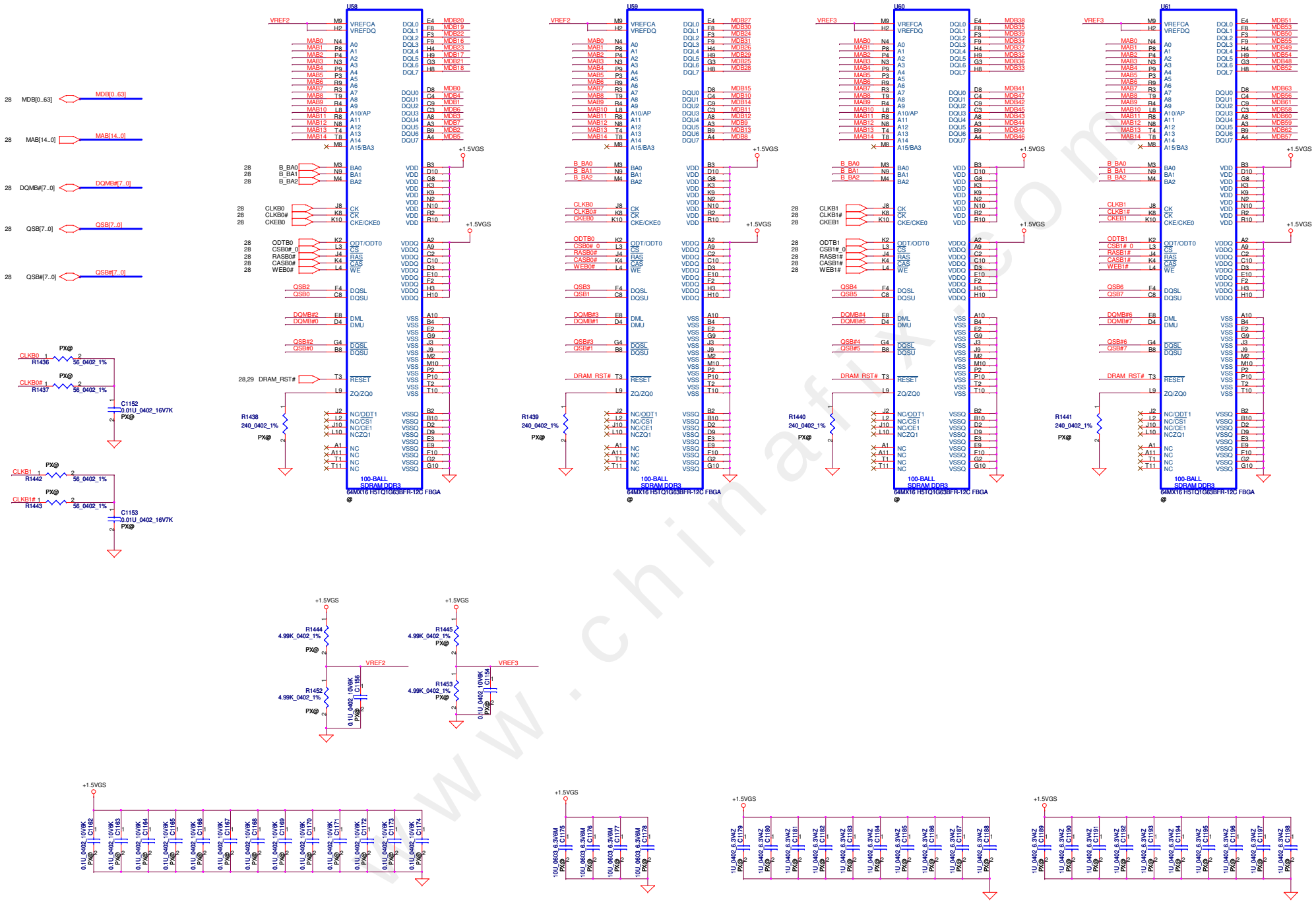

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B

Size	Document Number	Rev
C	QIQY2 LA6884P	1.0

Date: Wednesday, May 11, 2011 | Sheet 30 of 60

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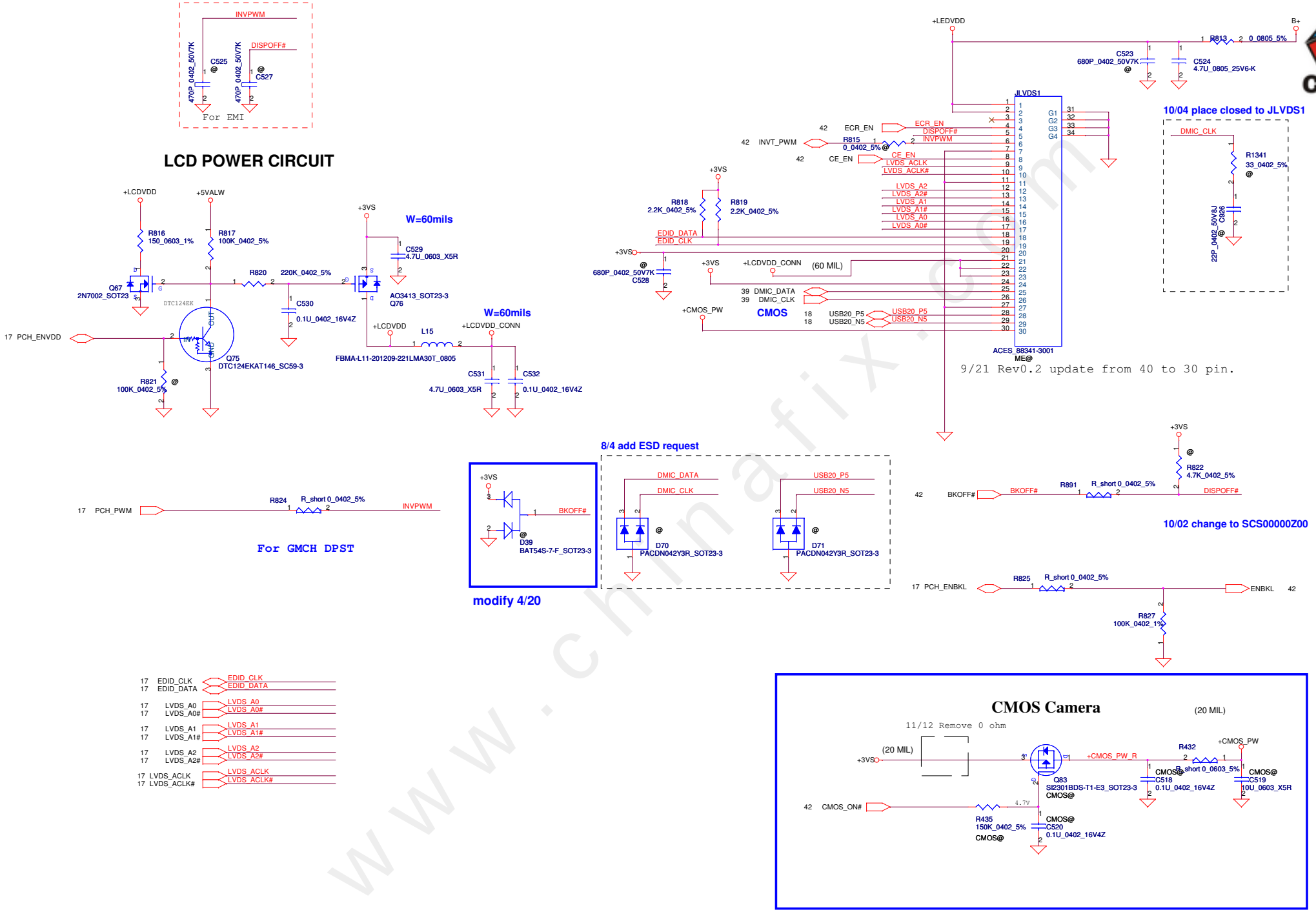

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
B	QIQY2 LA6884P	1.0

Date: Wednesday, May 11, 2011 | Sheet 31 of 60

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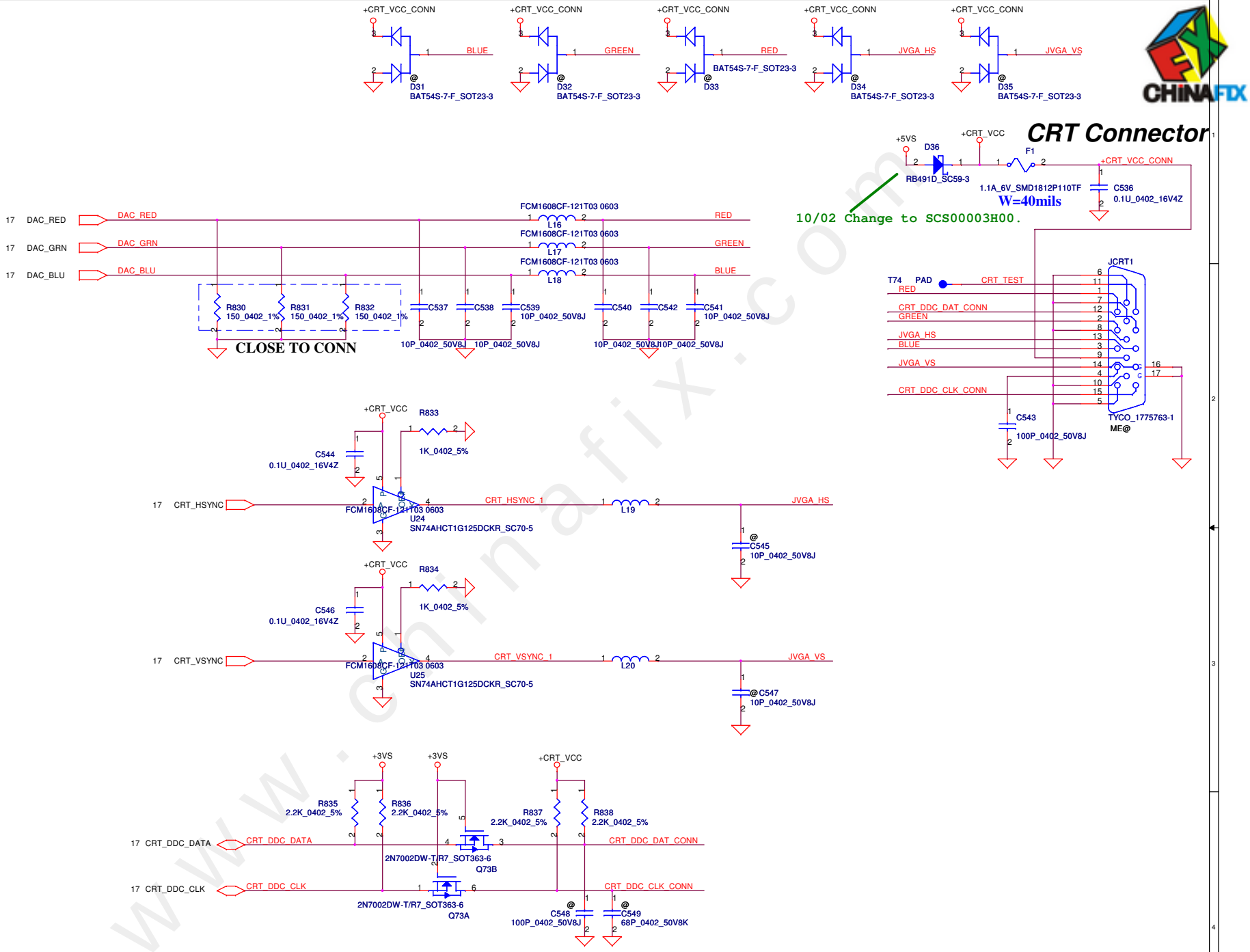
CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **QIQY2 LA6884P** | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 32 of 60

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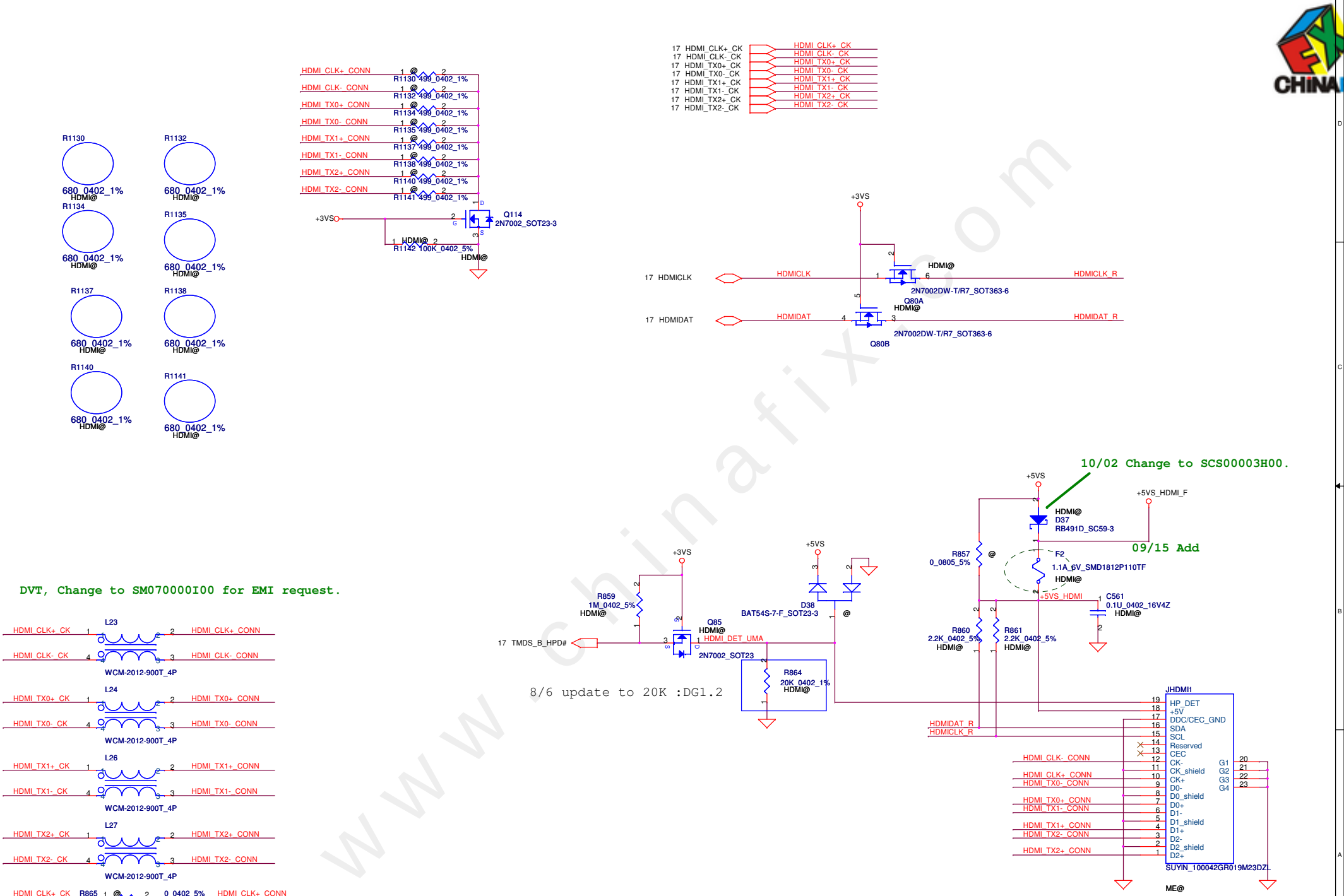

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics,Ltd.

Title: **HDMI CONN**

Size: Custom | Document Number: **QIQY2 LA6884P** | Rev: 1.0

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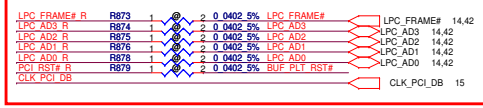
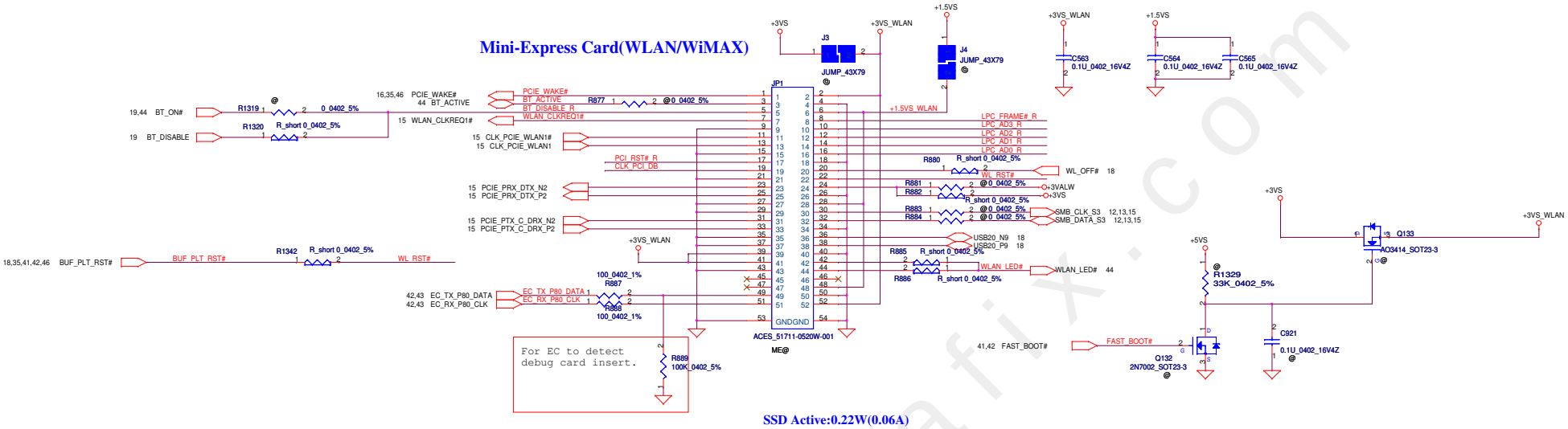
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

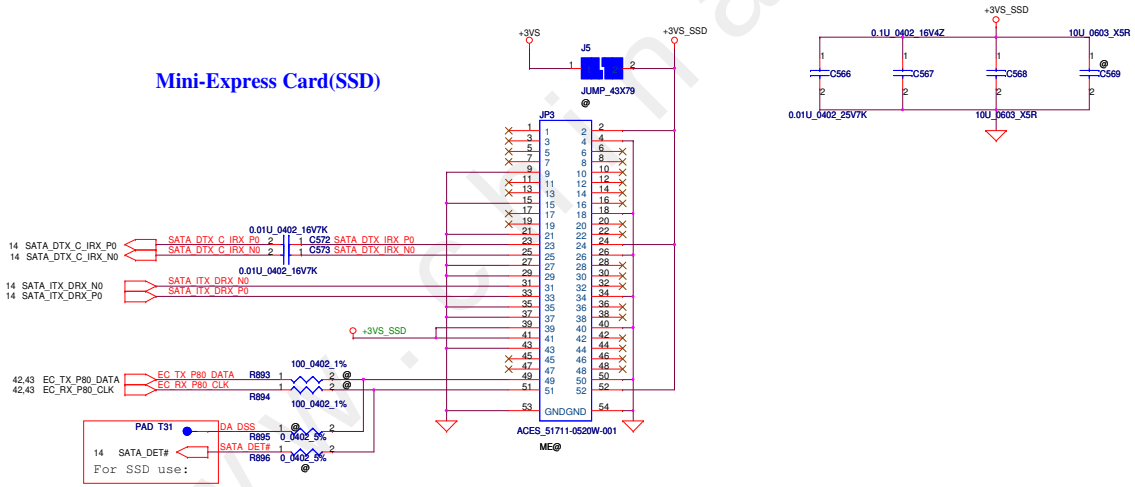


Mini-Express Card(WLAN/WiMAX)



SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)



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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: Mini-Card

Size | Document Number: QIQY2 LA6884P | Rev 1.0

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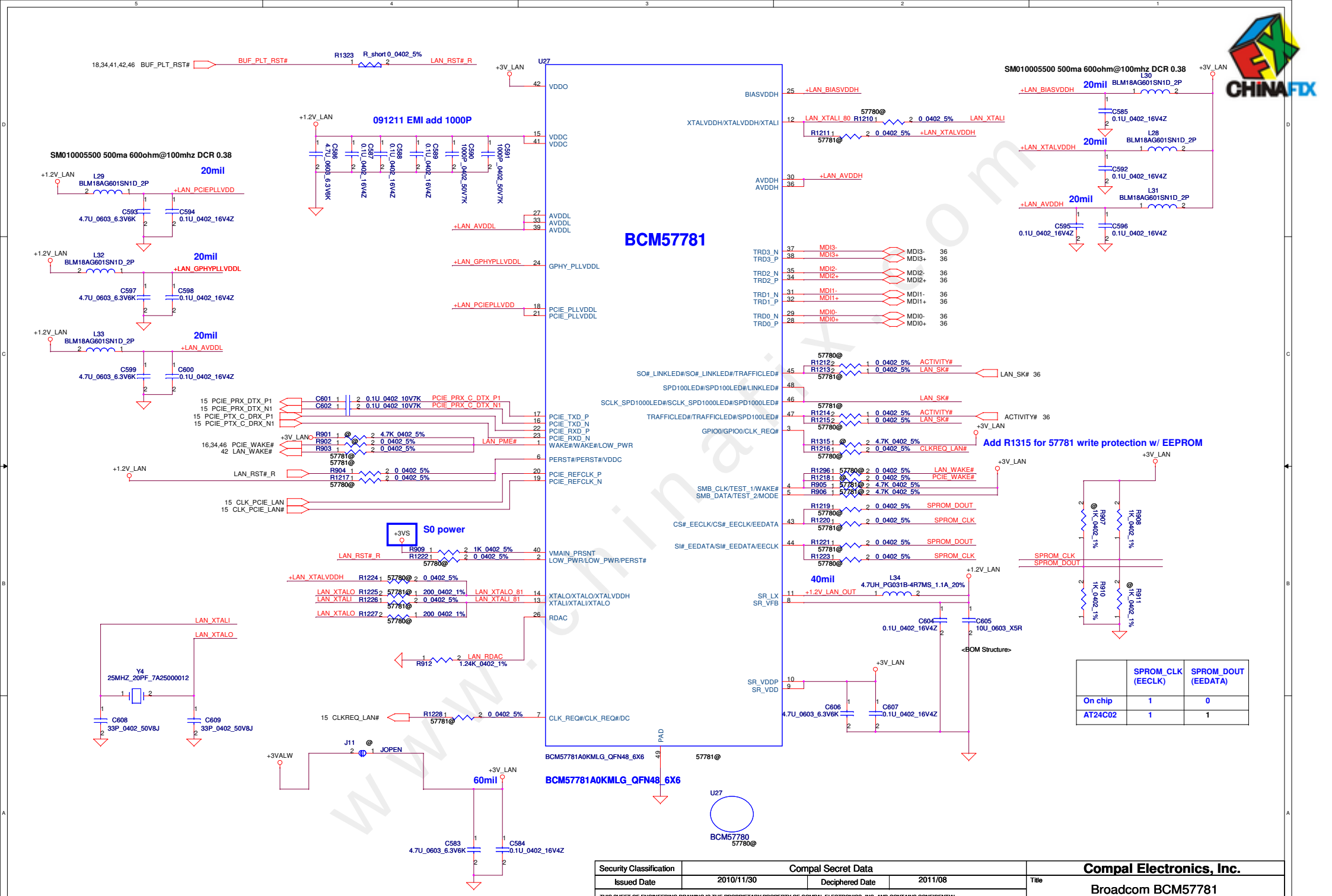

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: Broadcom BCM57781

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 35 of 60

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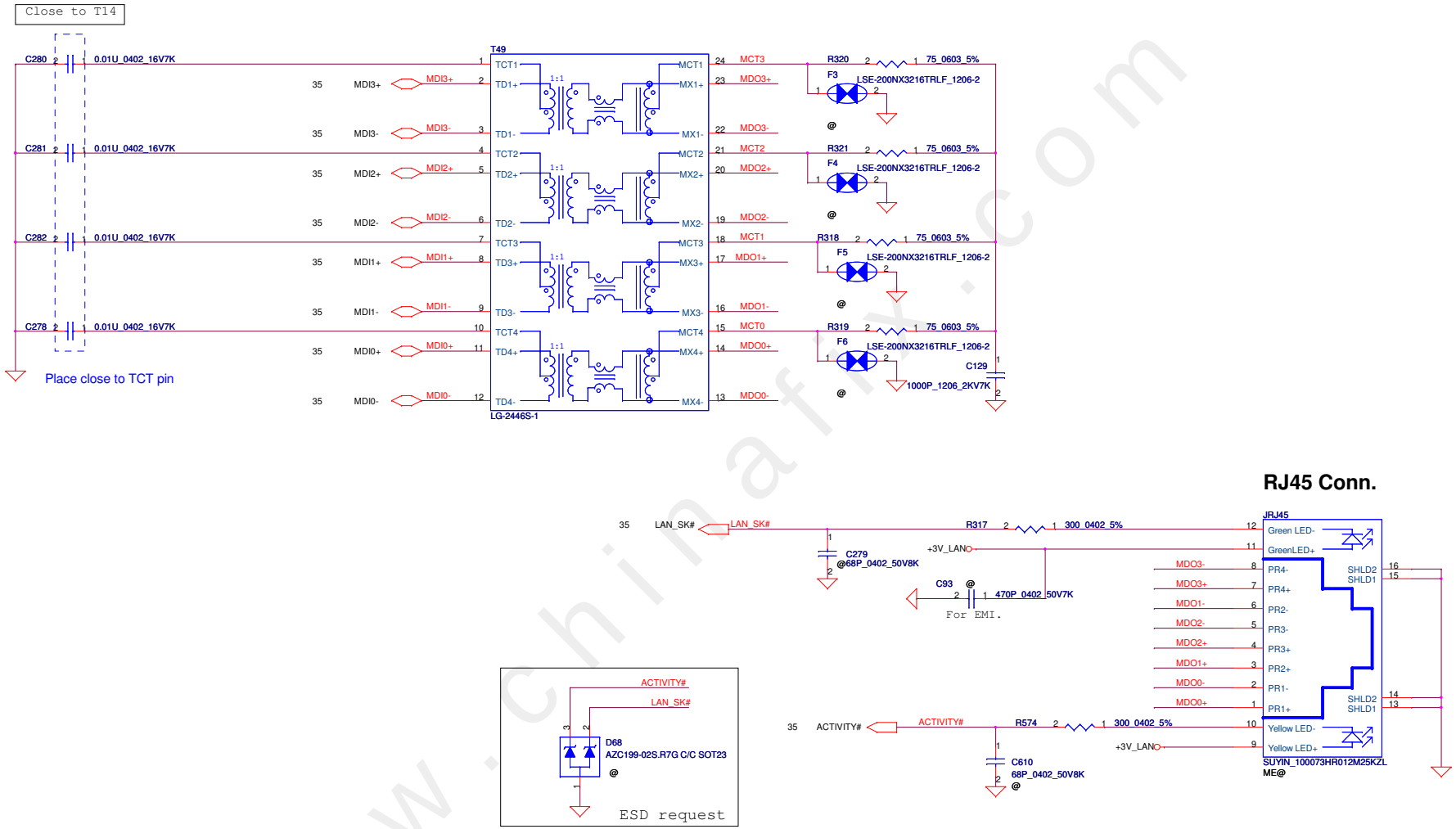

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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

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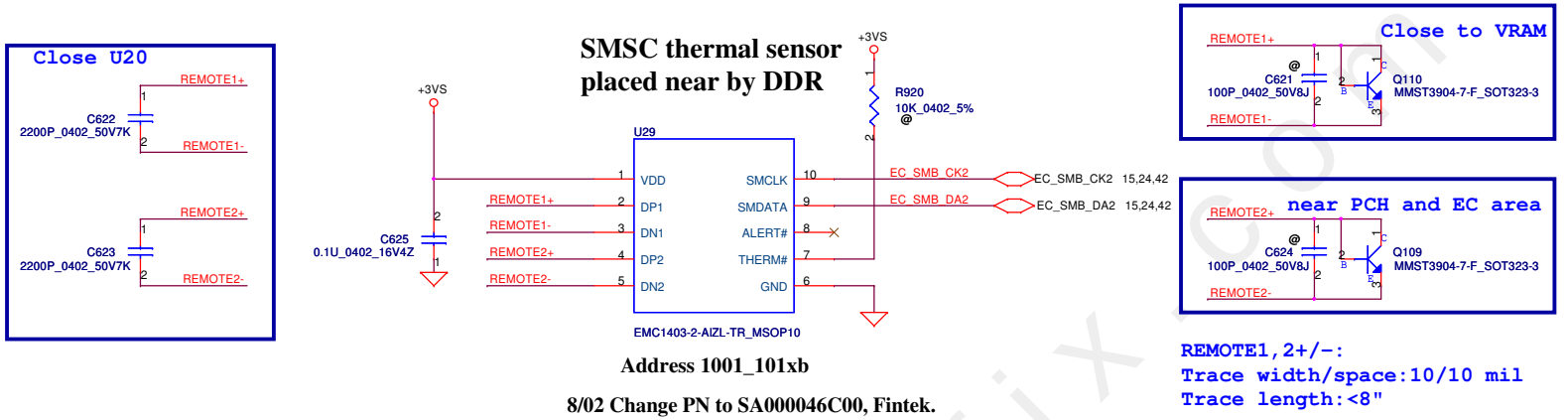
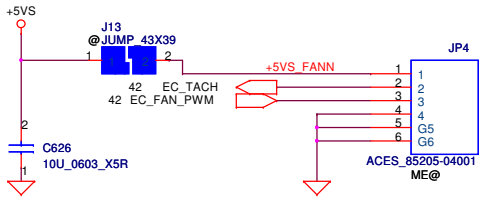


Address 1001_101xb

8/02 Change PN to SA000046C00, Fintek.

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



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Compal Electronics,Ltd.

Title: EMC1403_Thermal sensor/FAN

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

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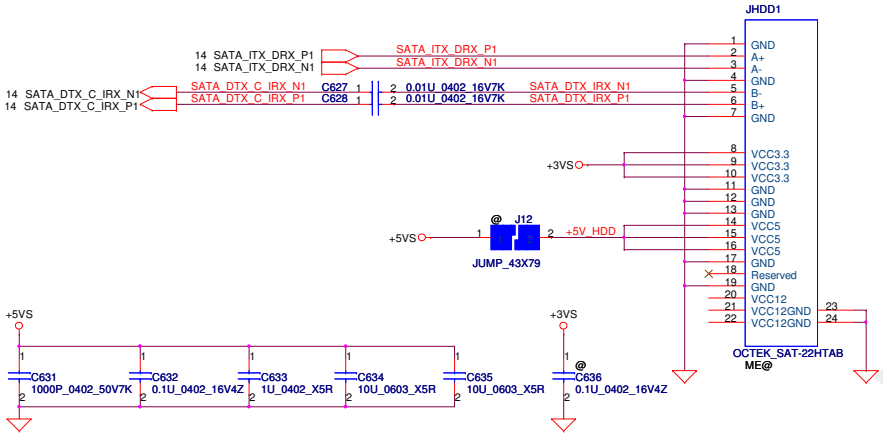
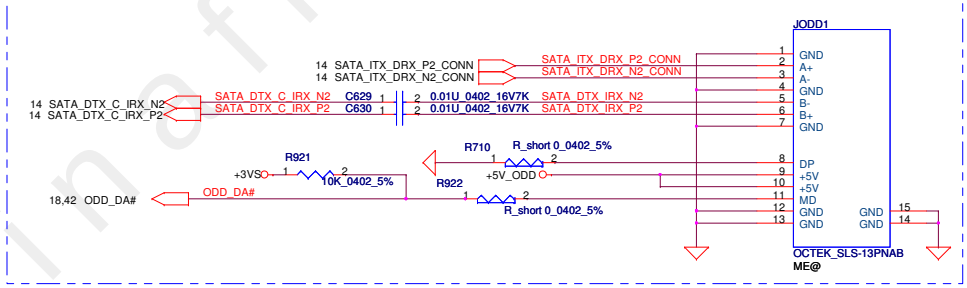
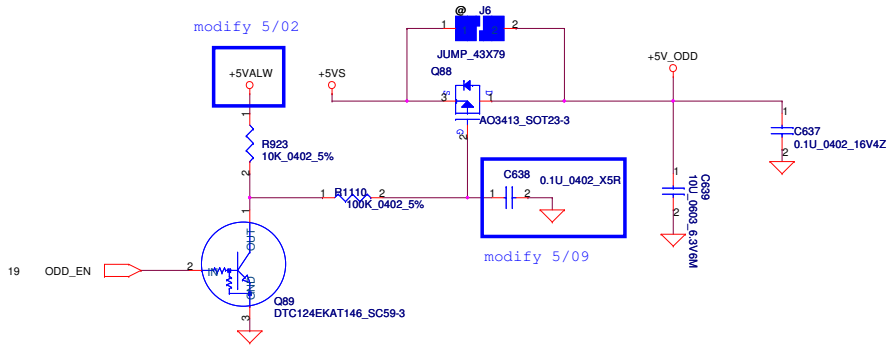
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: **HDD/ODD Connector**

Size	Document Number	Rev
B	QIQY2 LA6884P	1.0

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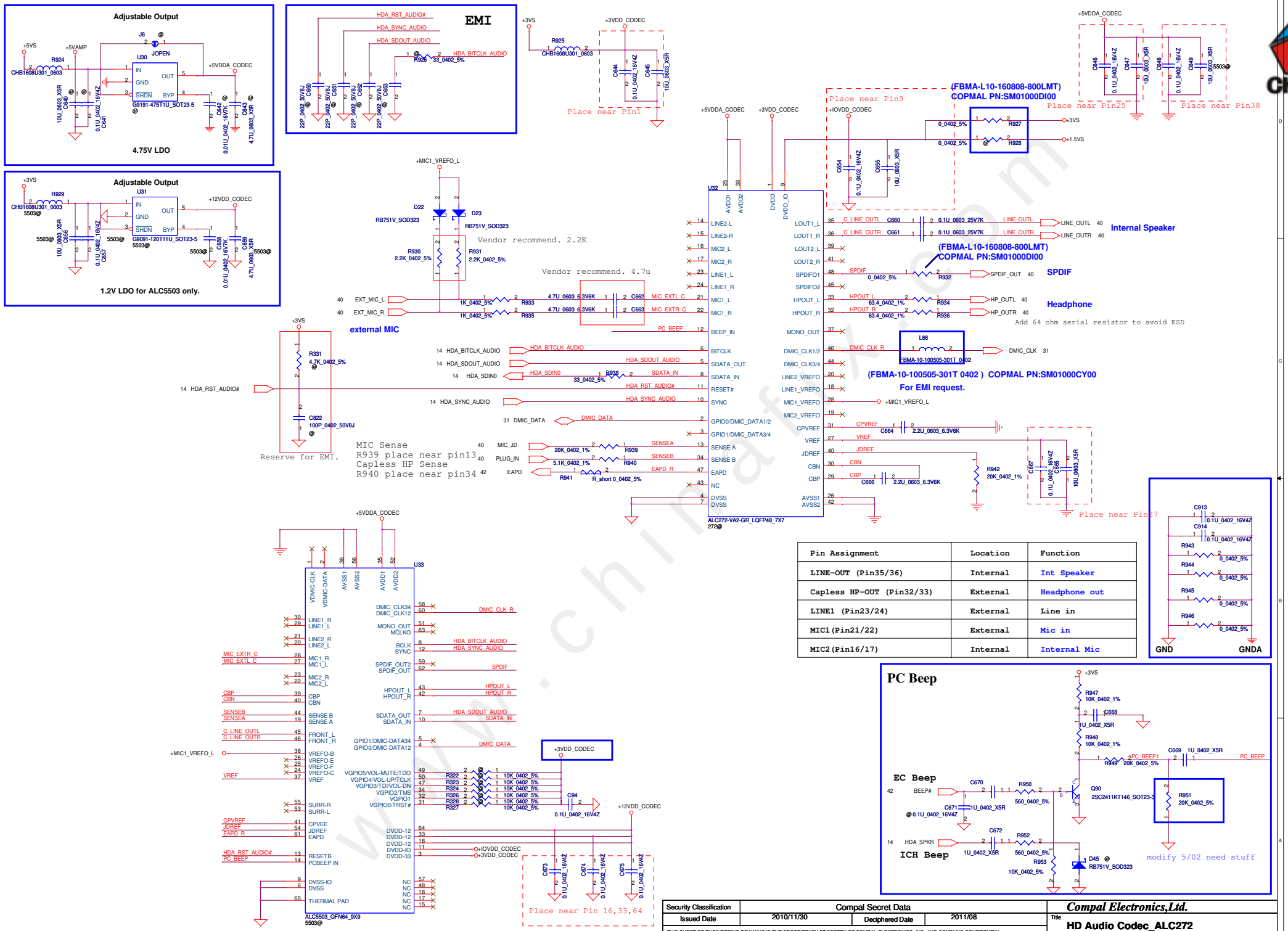

Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MIC2(Pin16/17)	Internal	Internal Mic

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics,Ltd.

Title: HD Audio Codec_ALC272

Size: C | Document Number: KIWB1/B2_LA4601P | Rev: 1.0

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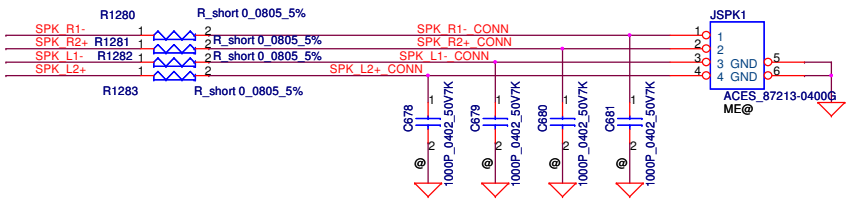
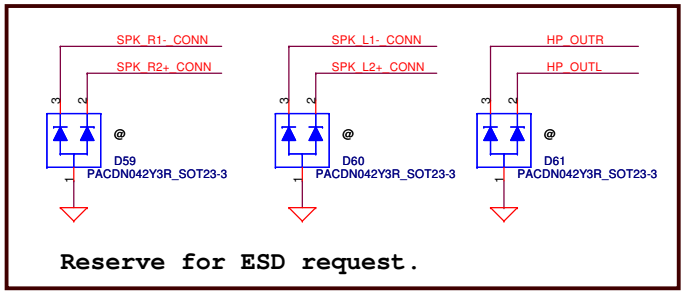
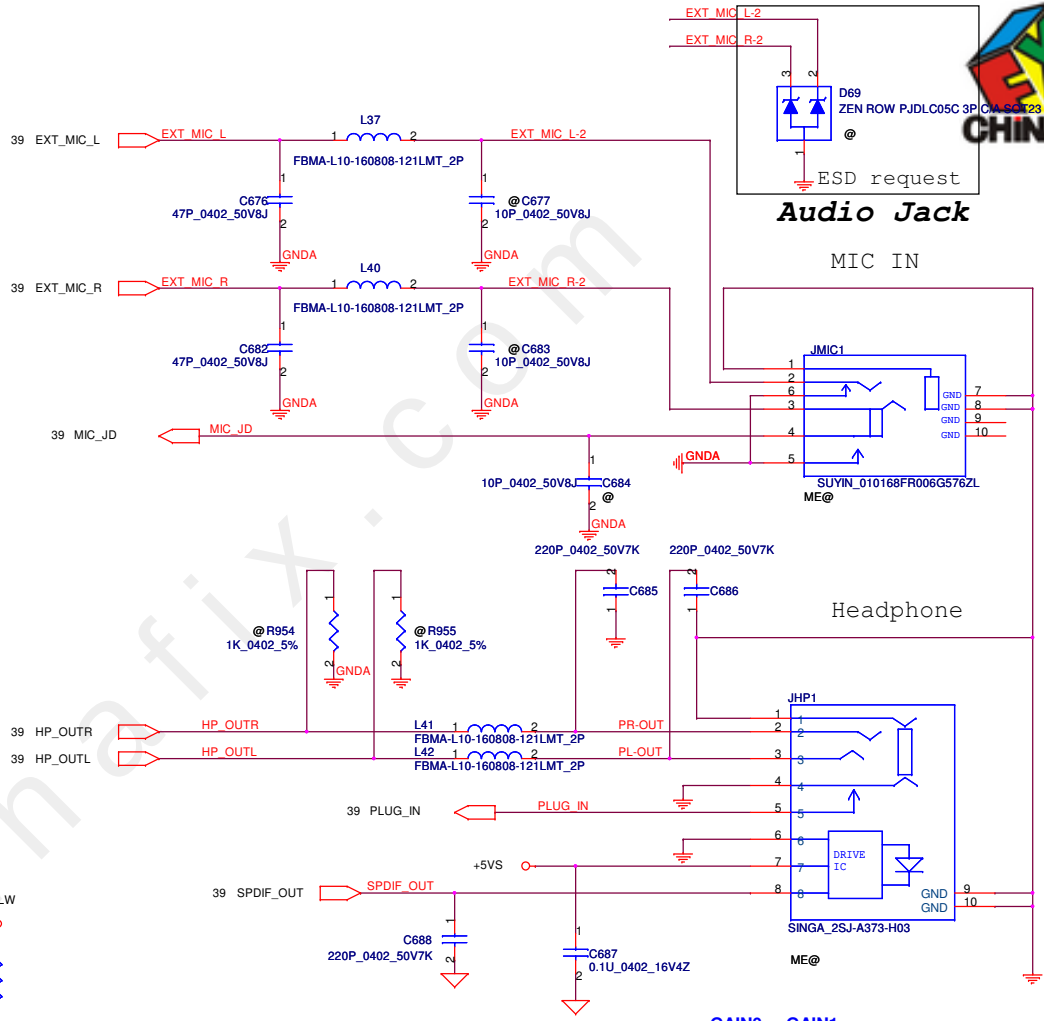
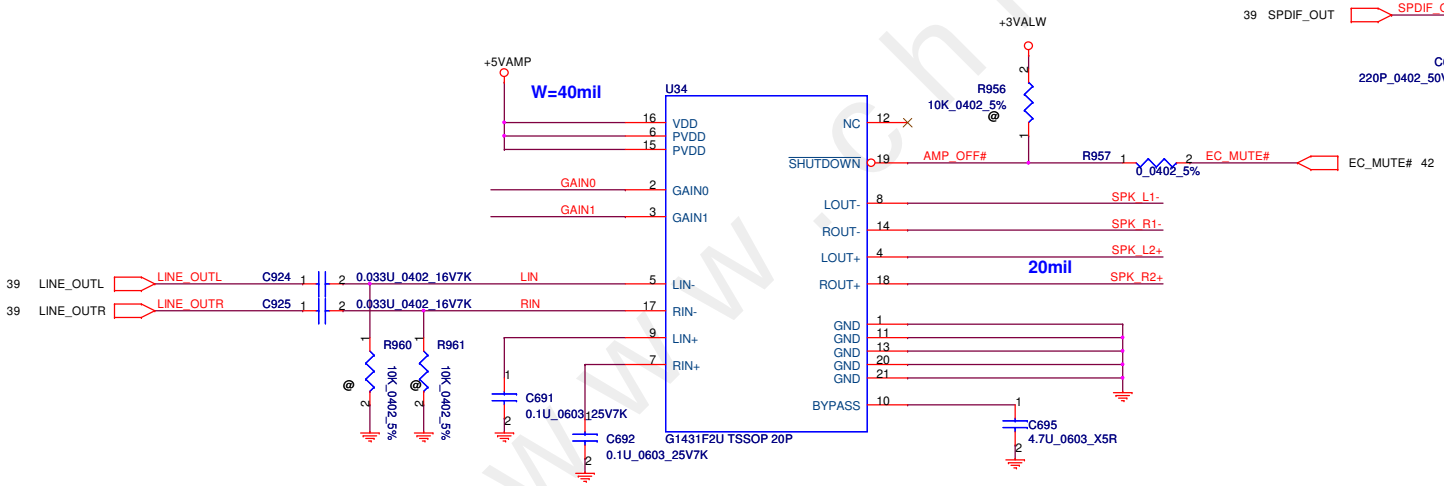
wide 20MIL

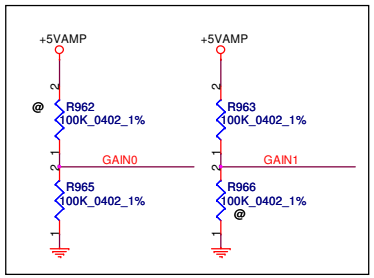








GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size: Custom | Document Number: KIWB1/B2_LA4601P | Rev: 1.0

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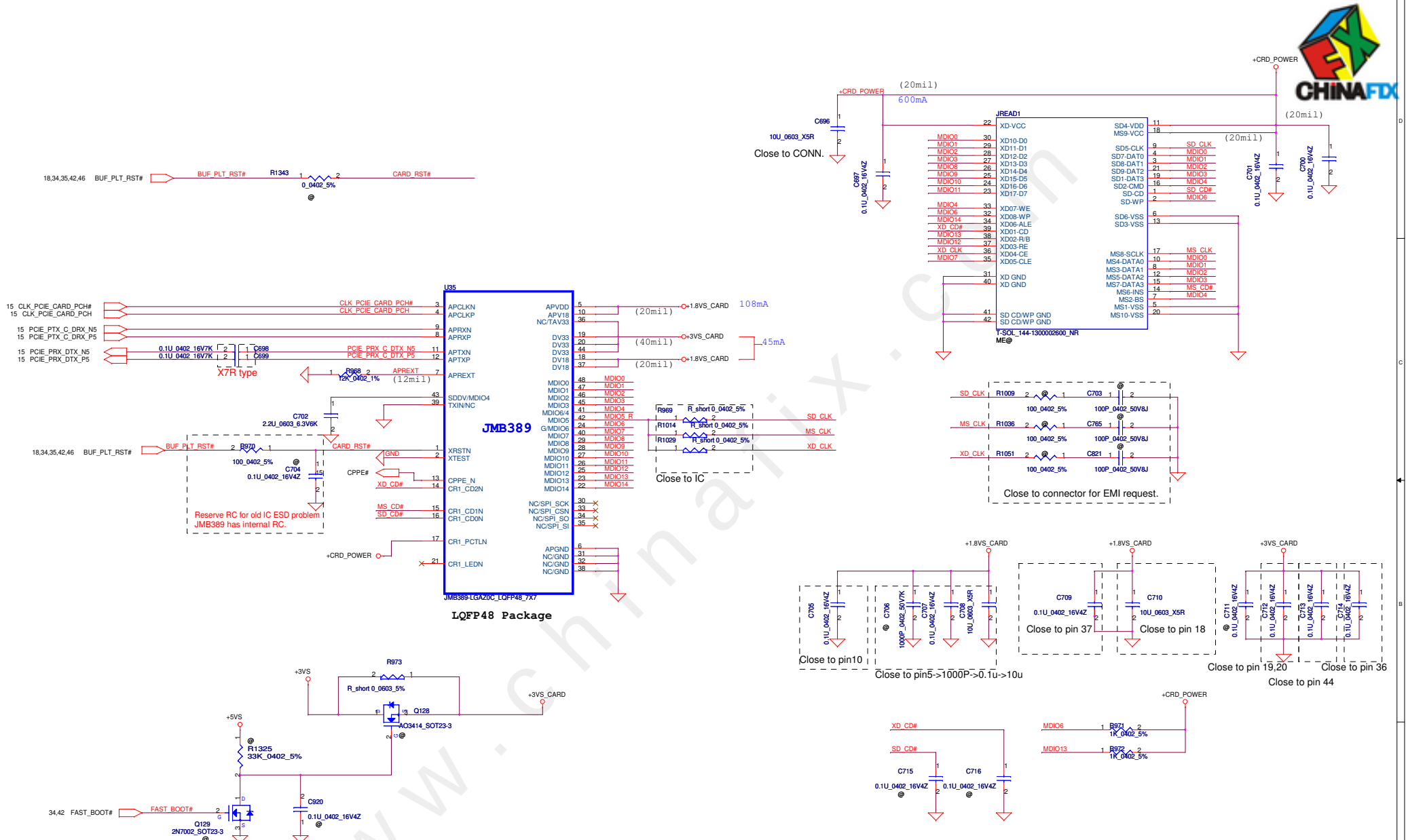

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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: Carder JMB389

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 41 of 60

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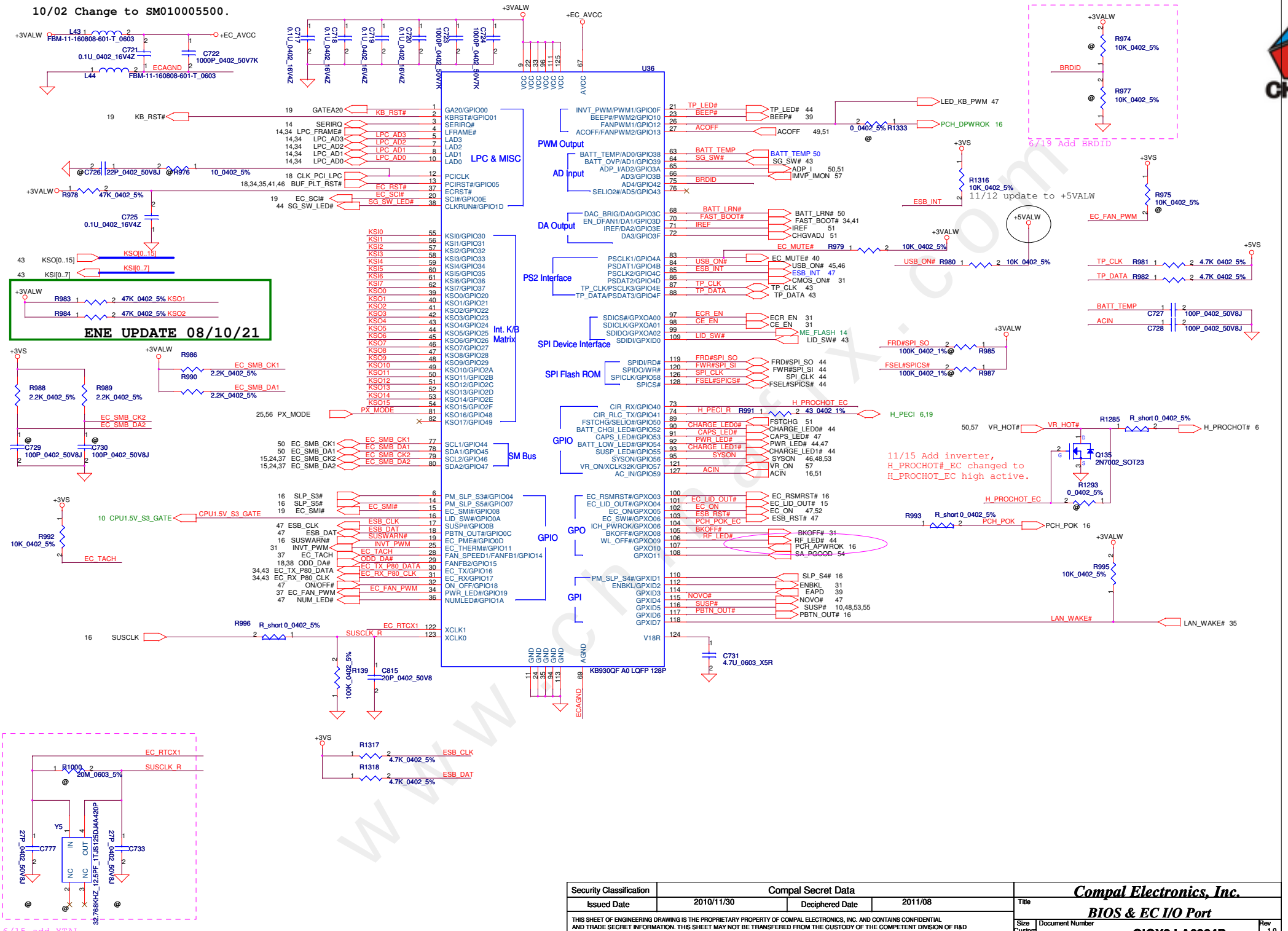
10/02 Change to SM010005500.



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **QIQY2 LA6884P** | Rev: 1.0

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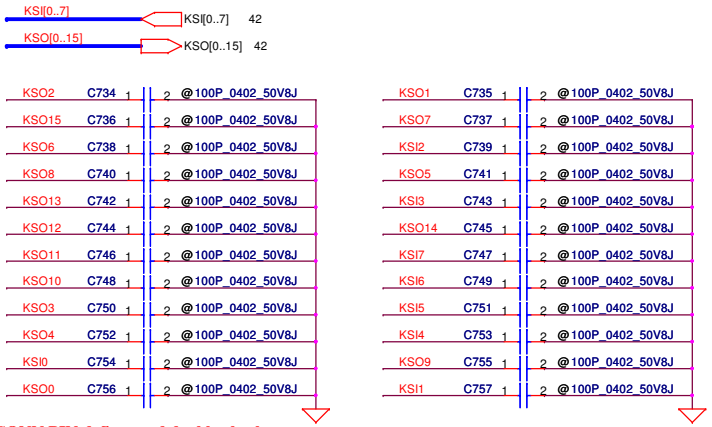
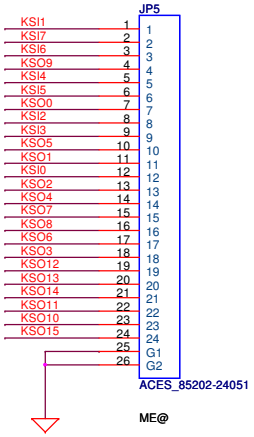
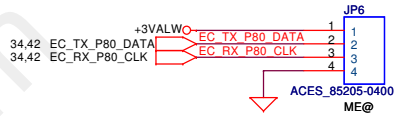
INT_KBD Conn.



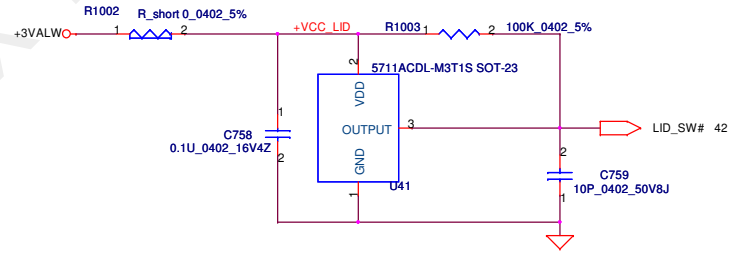
CONN PIN define need double check



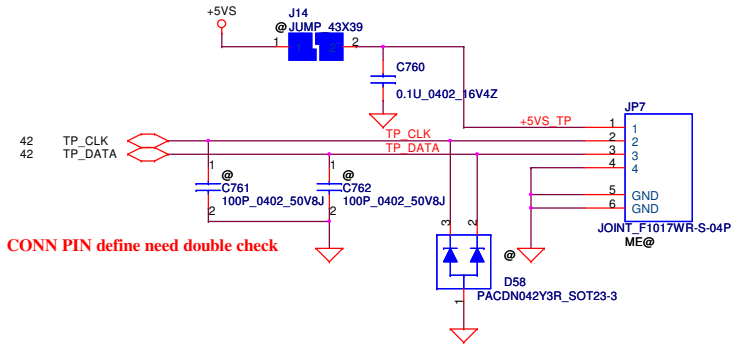
EC DEBUG PORT



Lid Switch

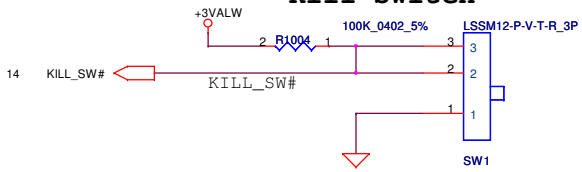


To TP/B Conn.



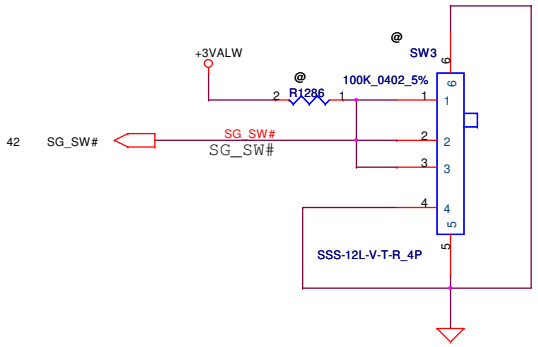
CONN PIN define need double check

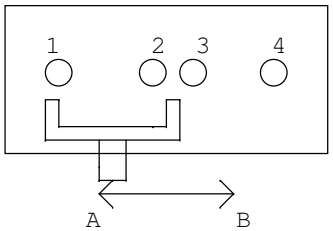
Kill Switch



Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON





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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: **KB /SW /LPC Debug Conn.**

Size: B | Document Number: **QIQY2 LA6884P** | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 43 of 60

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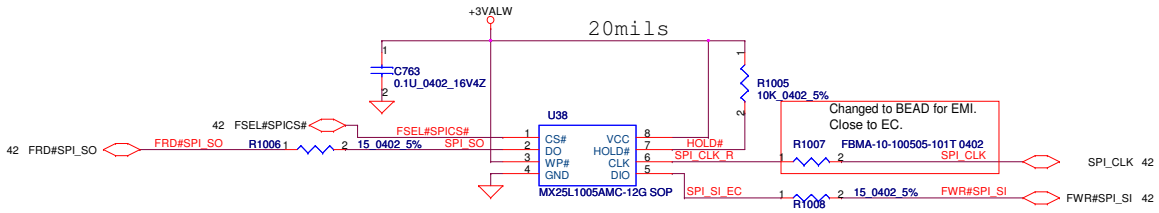
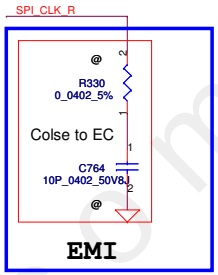
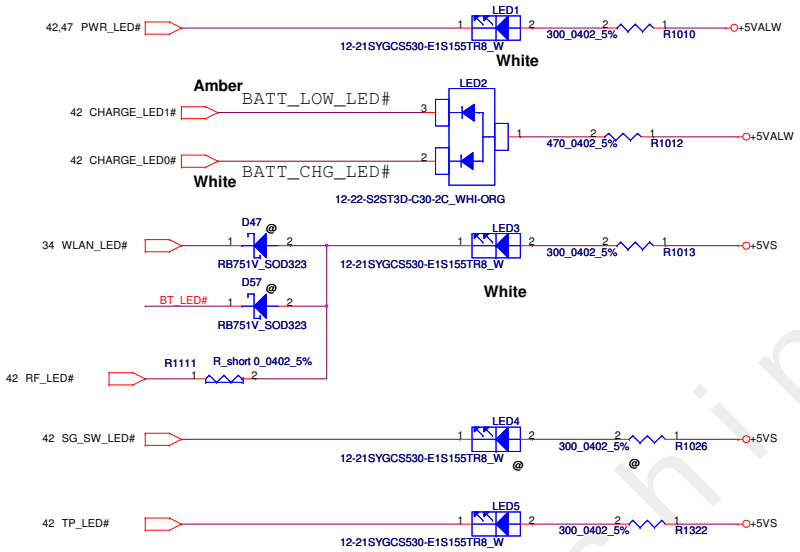
FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100

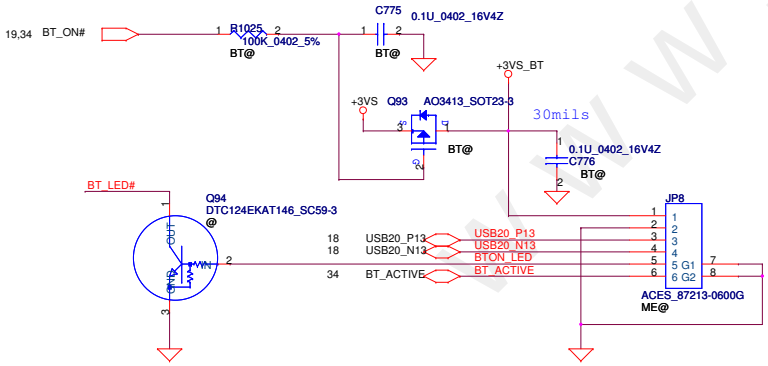


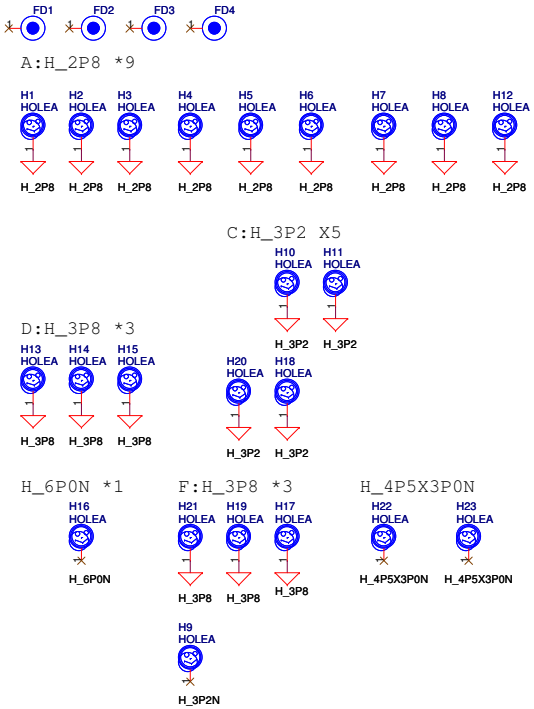


LED



BT MODULE CONN





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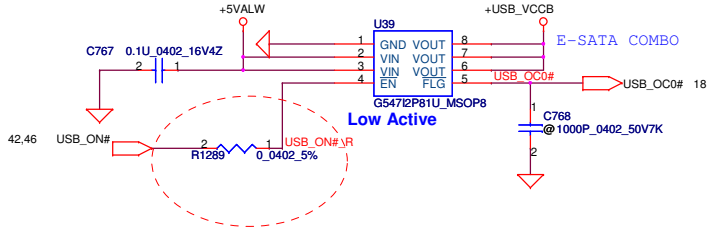
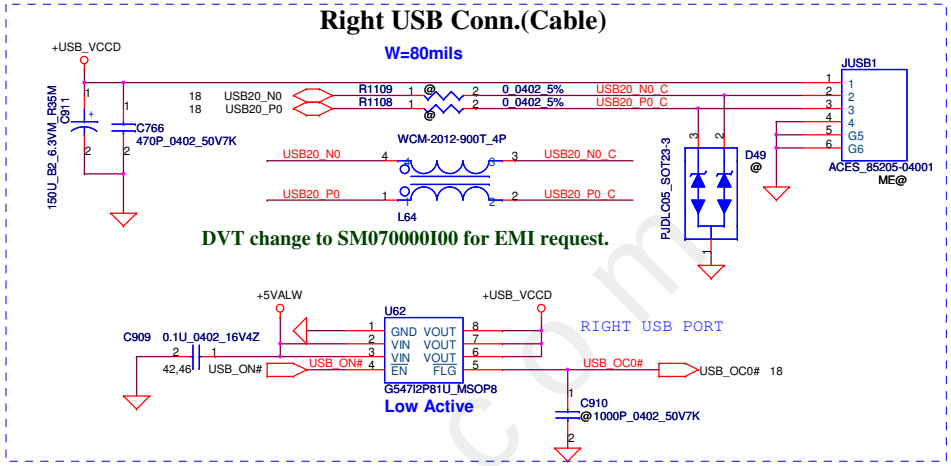
Compal Electronics, Inc.

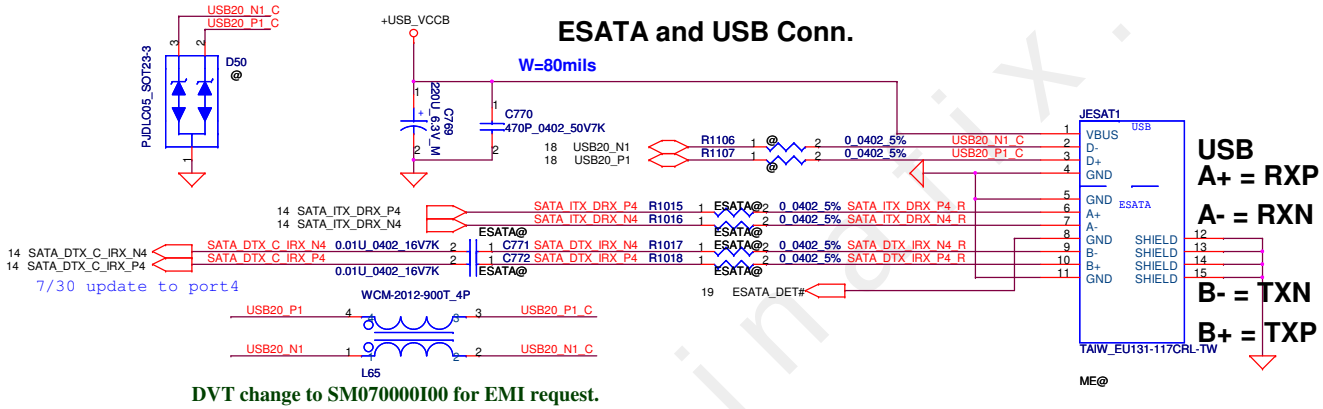
Title: **LED/EC SPI ROM/BT**

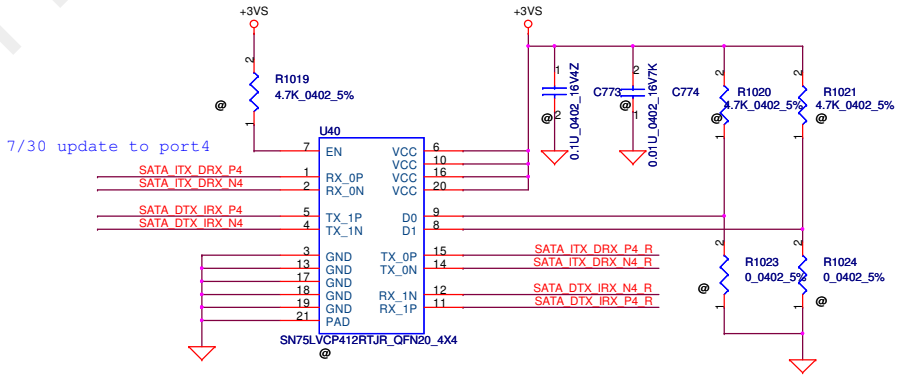
Size	Document Number	Rev
B	QIQY2 LA6884P	1.0

Date: Wednesday, May 11, 2011 Sheet 44 of 60









Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: USB ports/E-SATA

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 45 of 60

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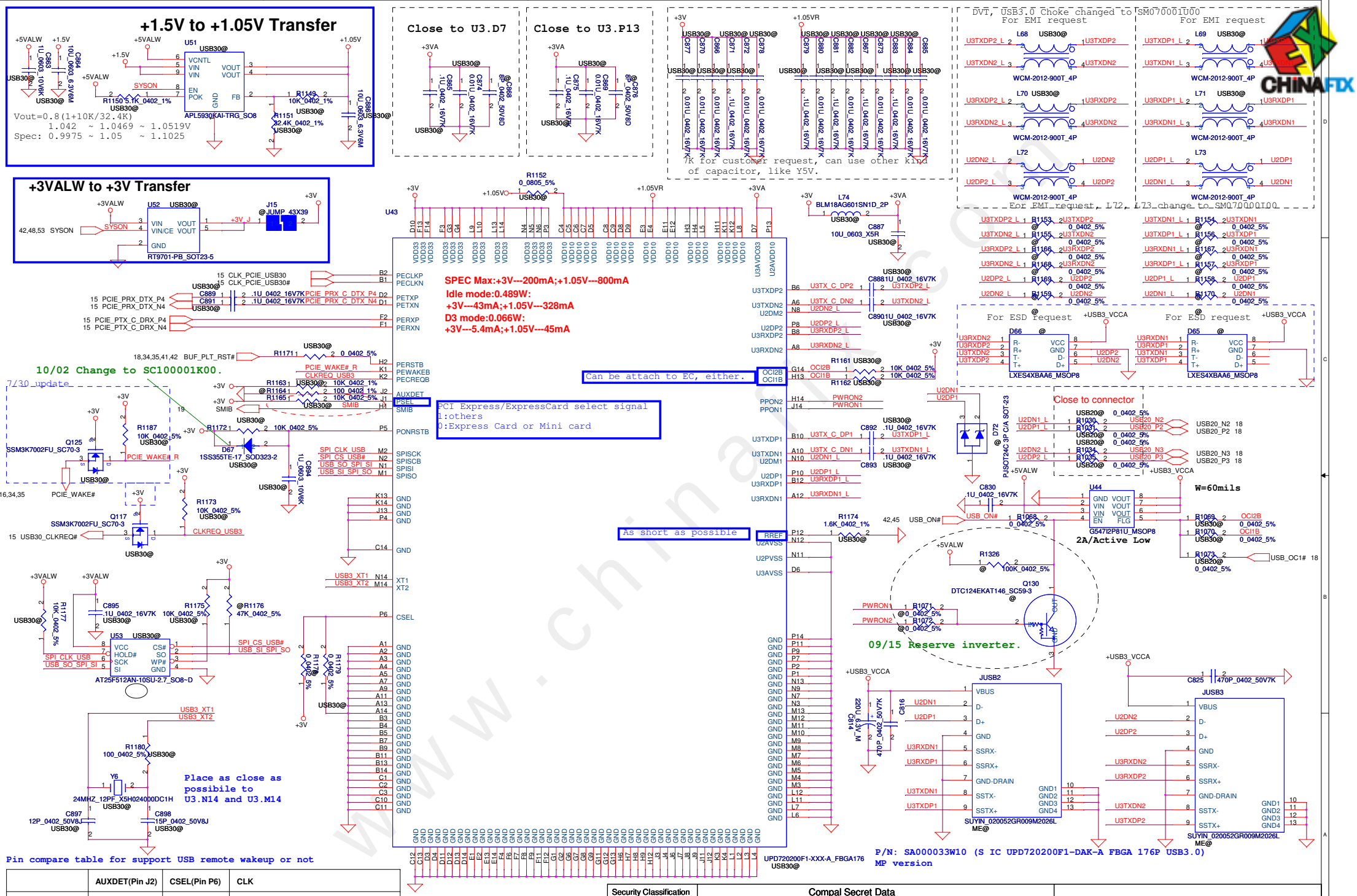

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

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Issued Date	2010/11/30	Deciphered Date	2011/08

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Title: USB3.0 PD720200

Size: Custom | Document Number | Rev 1.0

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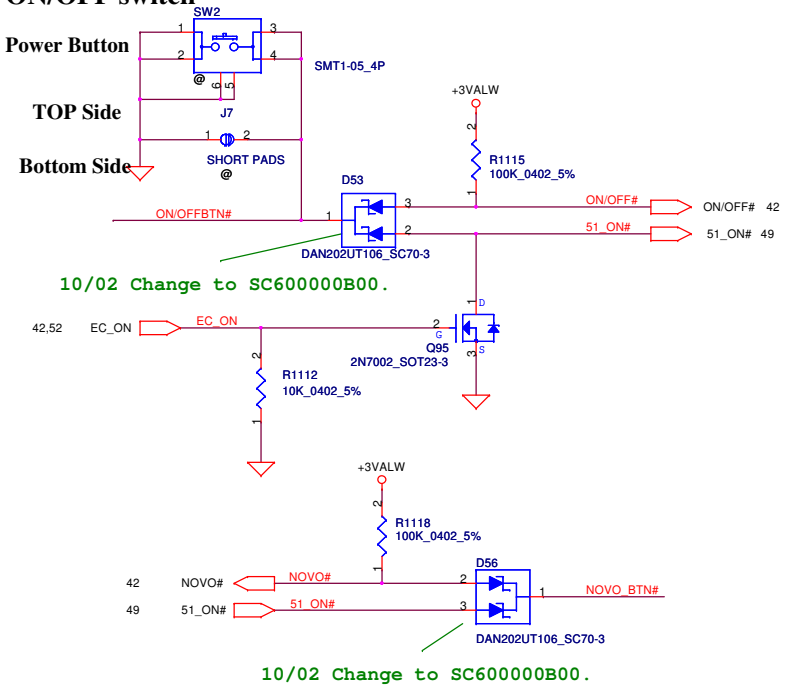
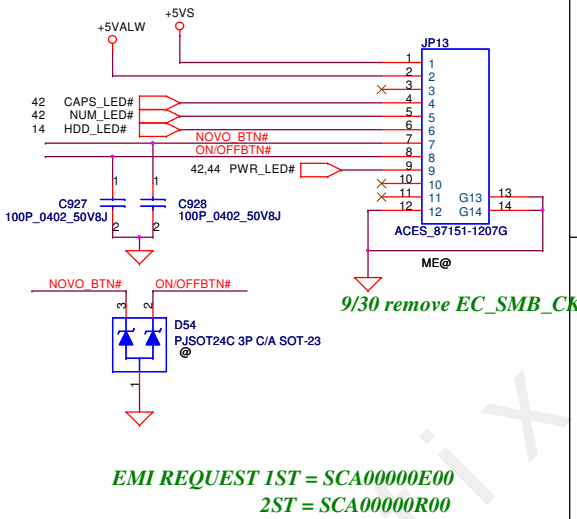
ON/OFF switch



Power Bottom Board Conn. 10pin

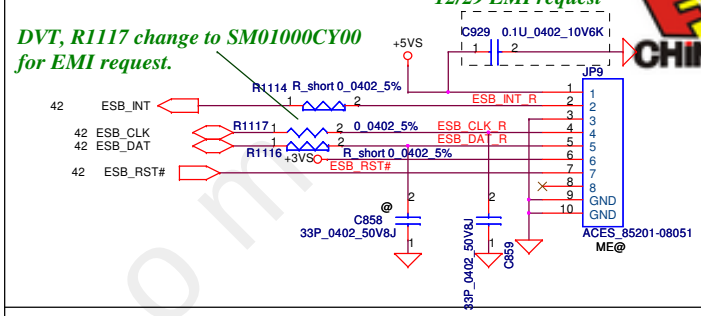


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

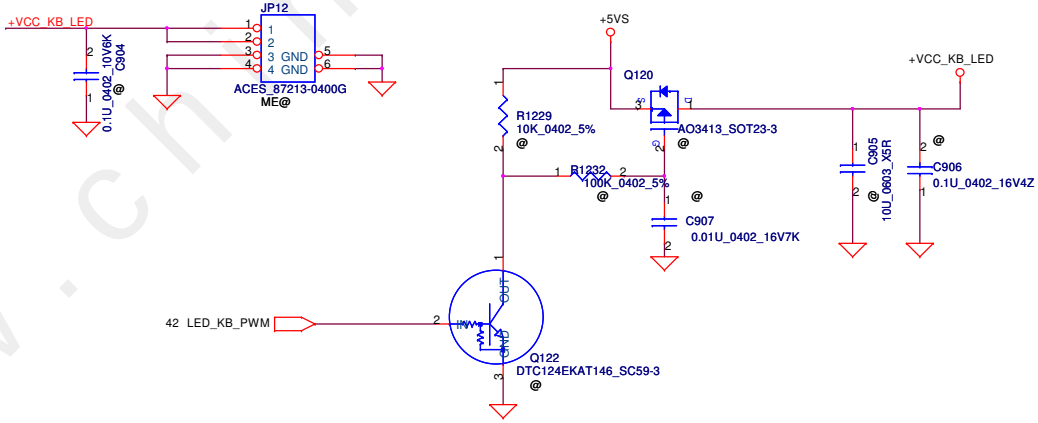
Silder Bar Board Mdule Conn. 6pin

12/29 EMI request

DVT, R1117 change to SM01000CY00 for EMI request.



KB Lighting CONN.4pin



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Compal Electronics,Ltd.

Title: other IO connector

Size: Custom | Document Number: QIQY2 LA6884P | Rev: 1.0

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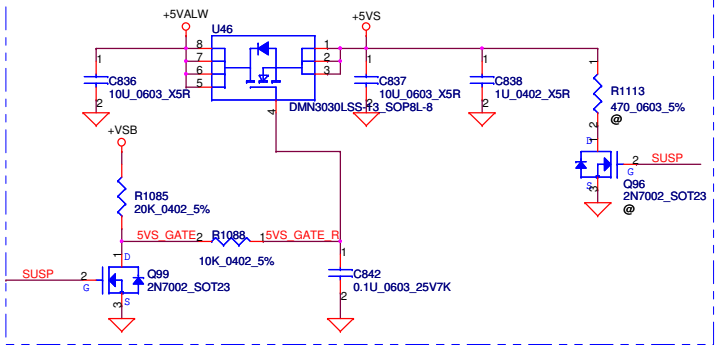
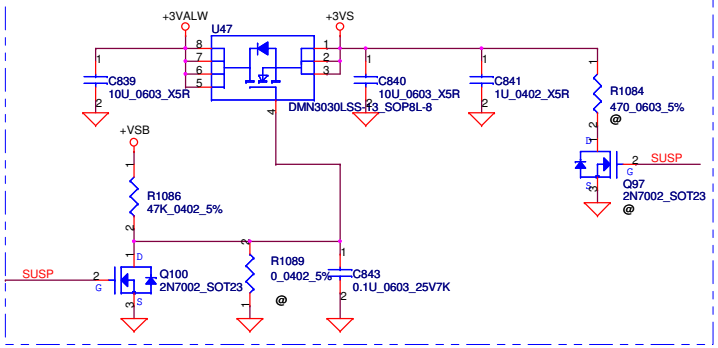
+5VALW TO +5VS

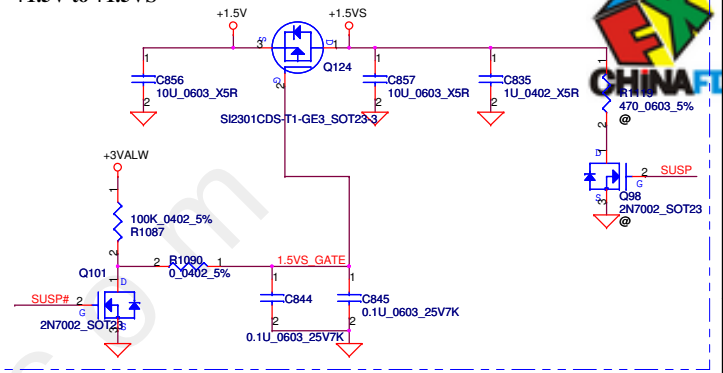


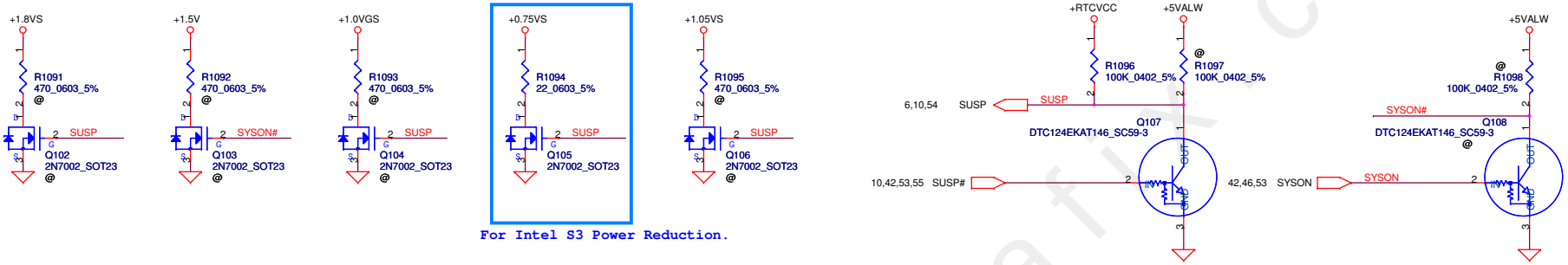
+3VALW TO +3VS



+1.5V to +1.5VS

5/10 change SI2301 to AP2301 GN-RH





For Intel S3 Power Reduction.

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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: DC Interface

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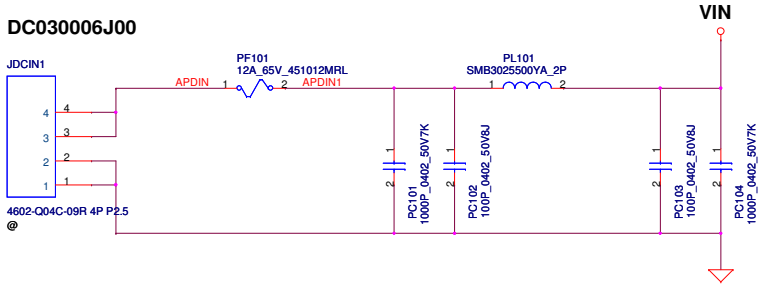
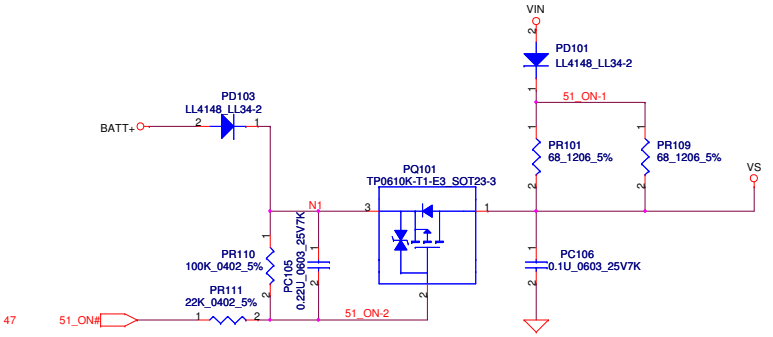
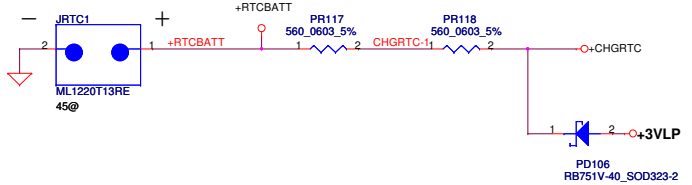
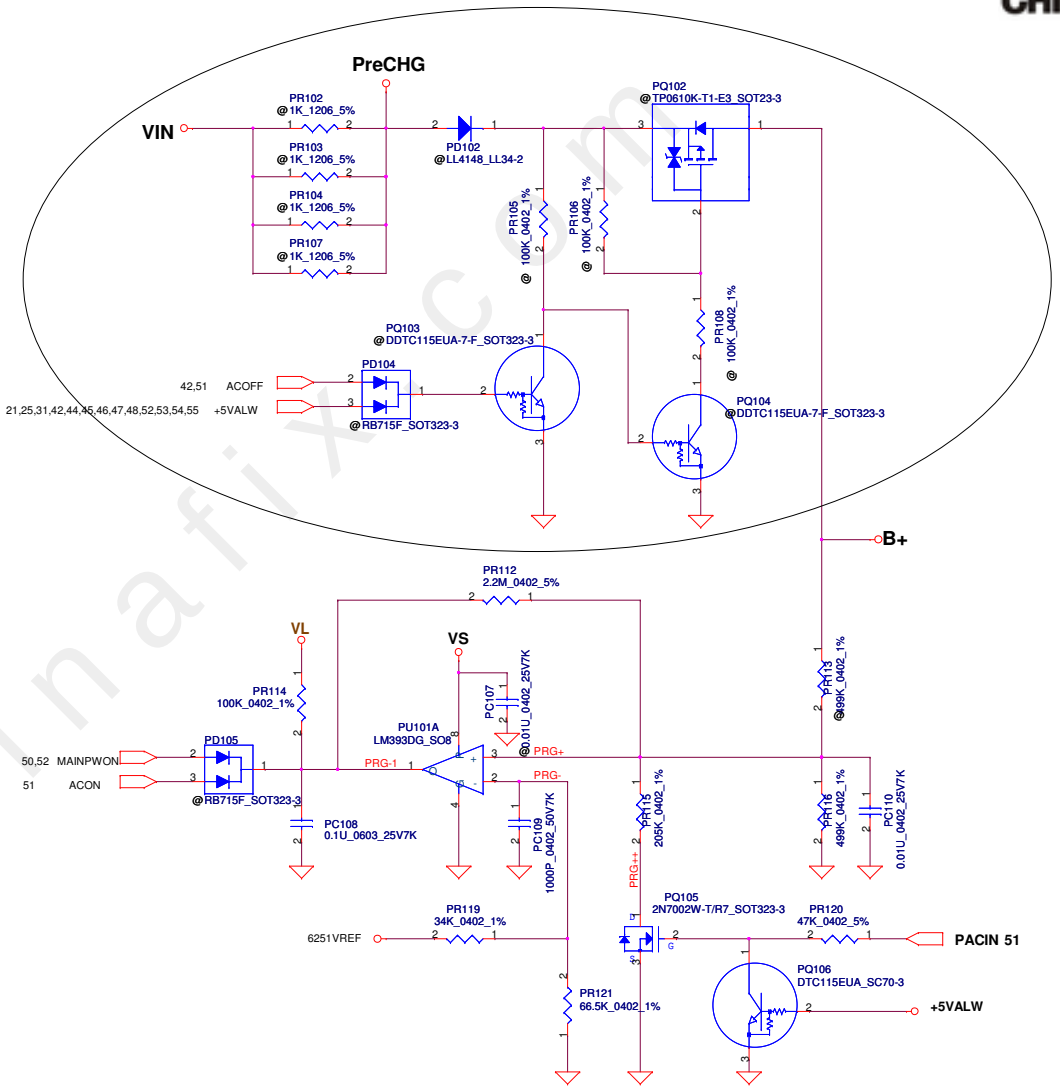
DC030006J00







Precharge detector
15.97V/14.84V FOR
ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: ***PWR DCIN / Vin Detector /Pre-charge***

Size: Custom | Document Number: **PIQY0/Y1** | Rev: 1.0

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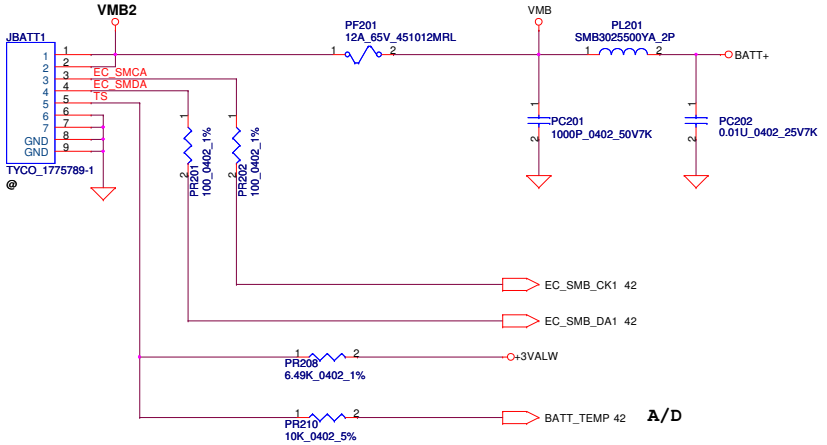
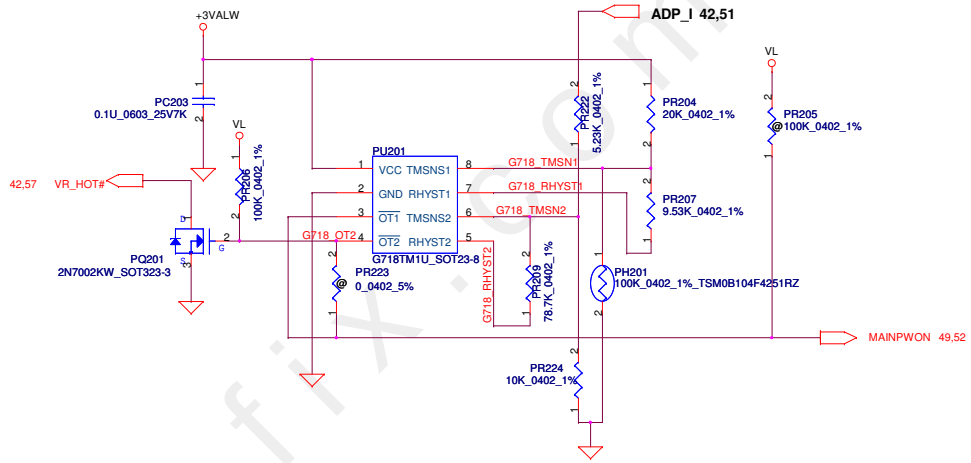
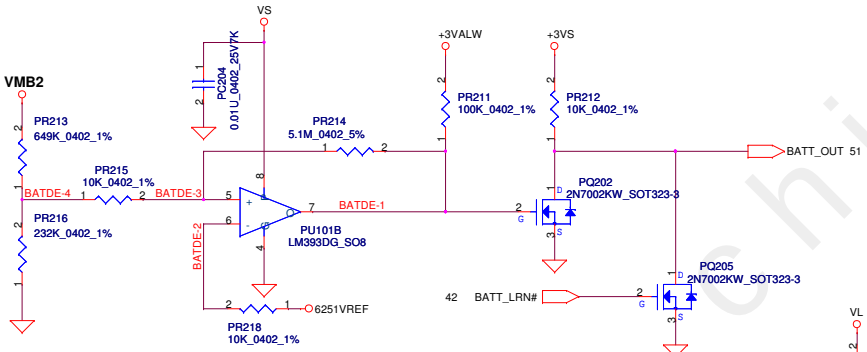
PH201 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

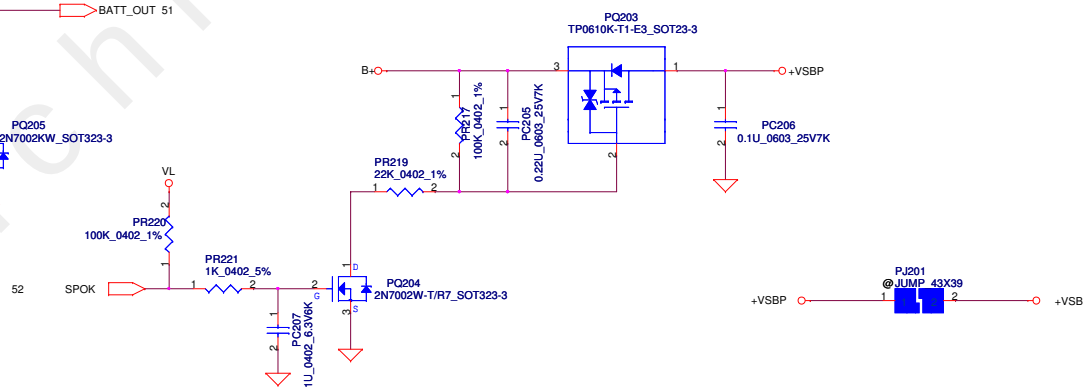




PR209	
90W :	20.5K ohm
120W :	78.7K ohm

PR222	
90W :	6.65K ohm
120W :	5.23K ohm





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Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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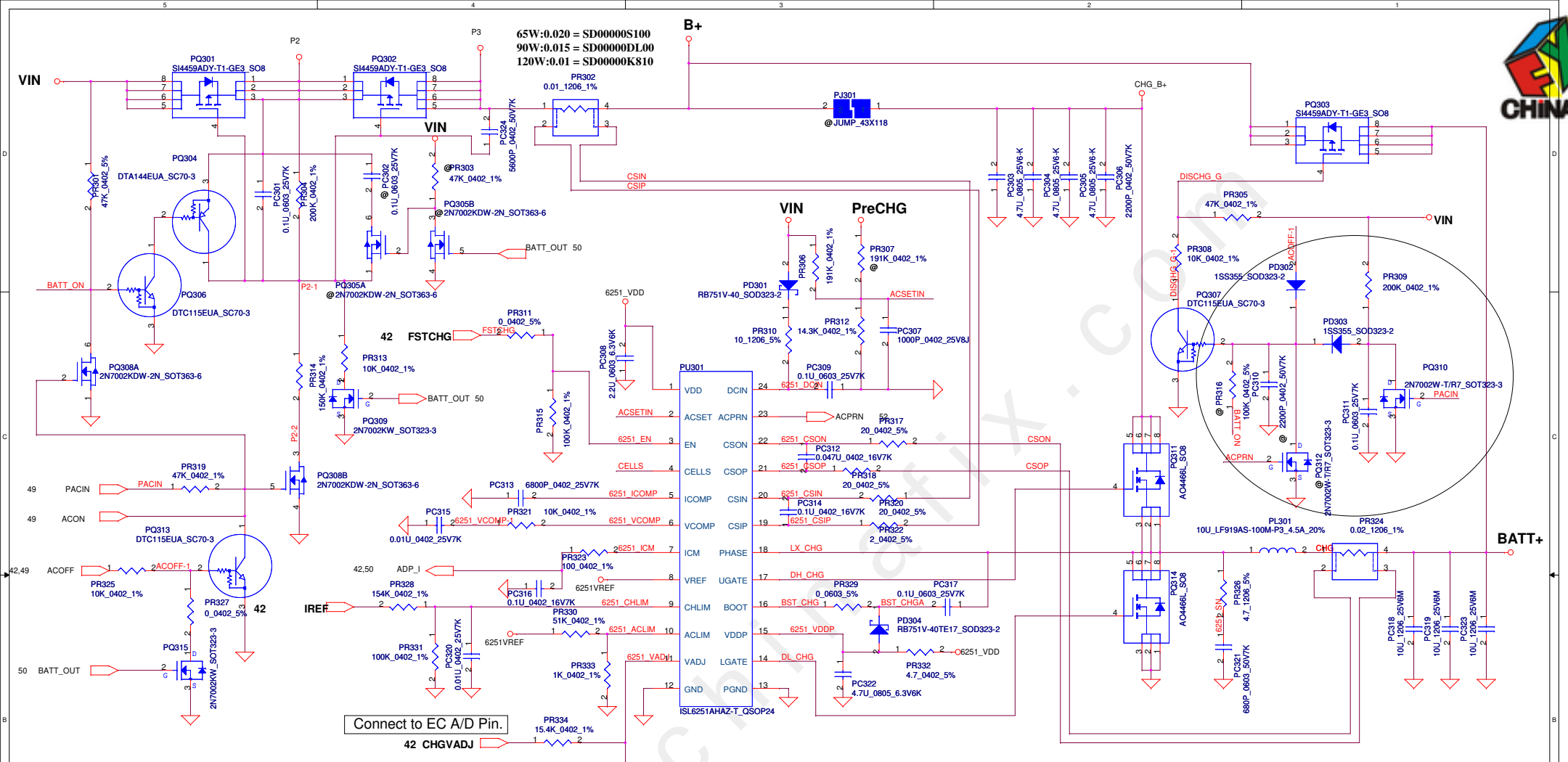
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 50 of 63



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

65W Adapter
Vaclim=2.39*(1.96K/(1.96K+16.9K))=0.2484V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2484V, Iinput=2.76A

90W Adapter
Vaclim=2.39*(2.87K/(2.87K+16.9K))=0.347V
Iinput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.347V, Iinput=3.82A

120W Adapter
Vaclim=2.39*(1K/(1K+50K))=0.047V
Iinput=(1/0.01)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.047V, Iinput=5.1A

65W : PR330=16.9K, PR333=1.96K
90W : PR330=16.9K, PR333=2.87K
120W : PR330=50K, PR333=1K

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: PIQY0/Y1 | Rev 1.0

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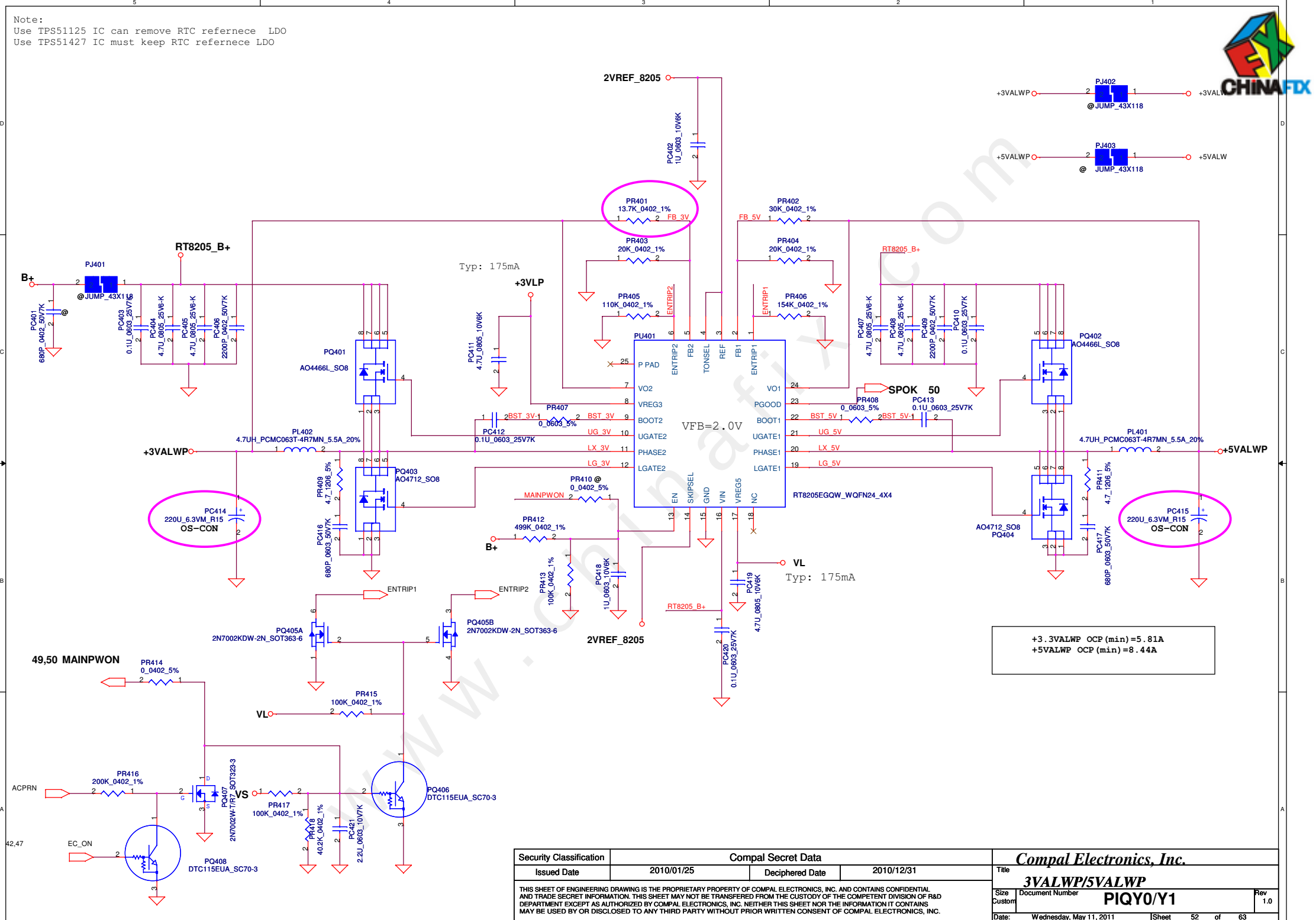
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 52 of 63

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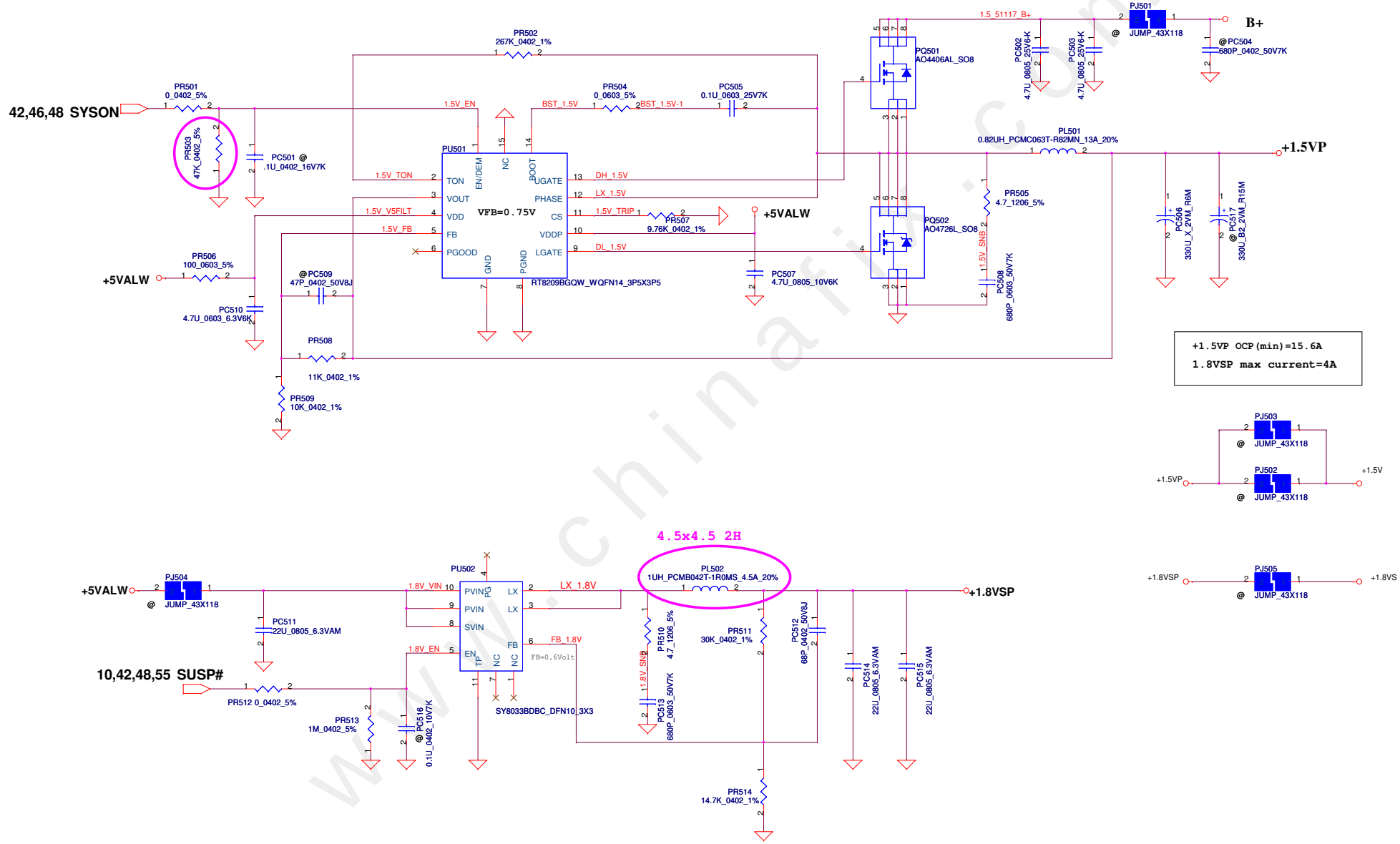

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size: Custom | Document Number: **PIQY0/Y1** | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 53 of 63

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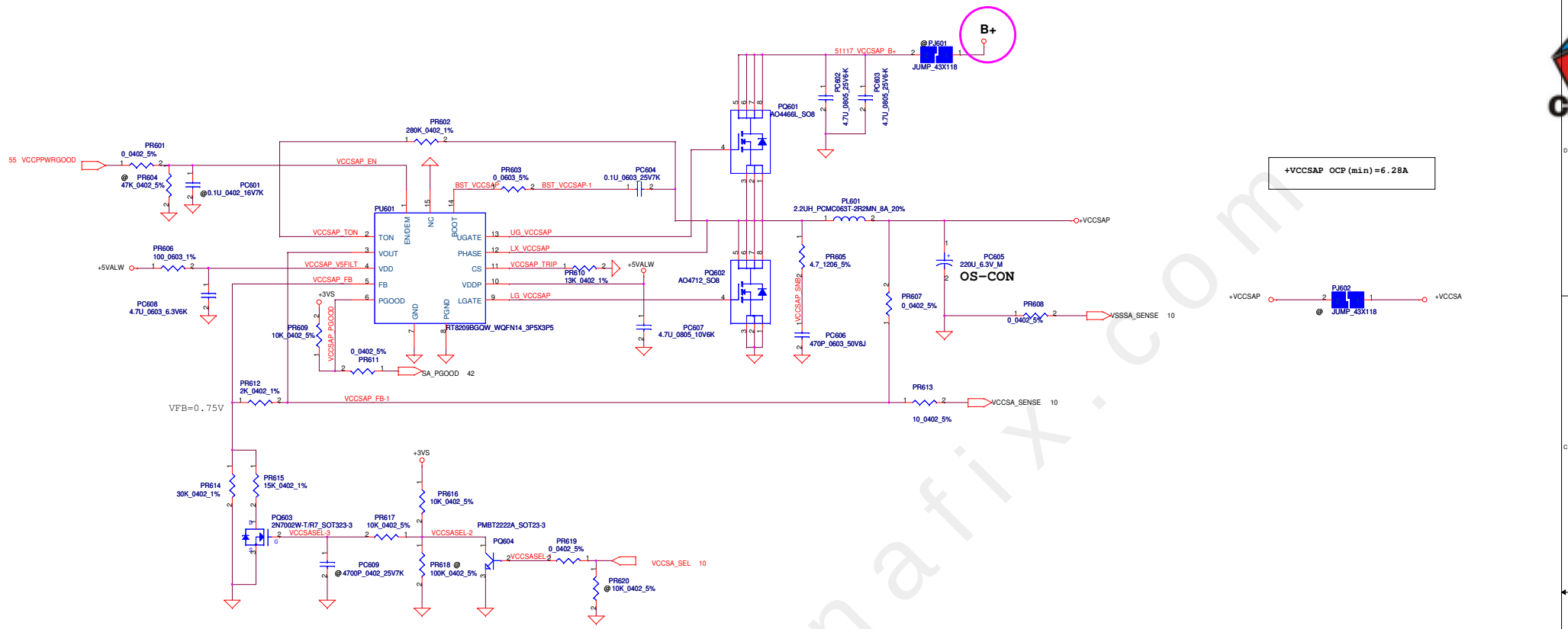
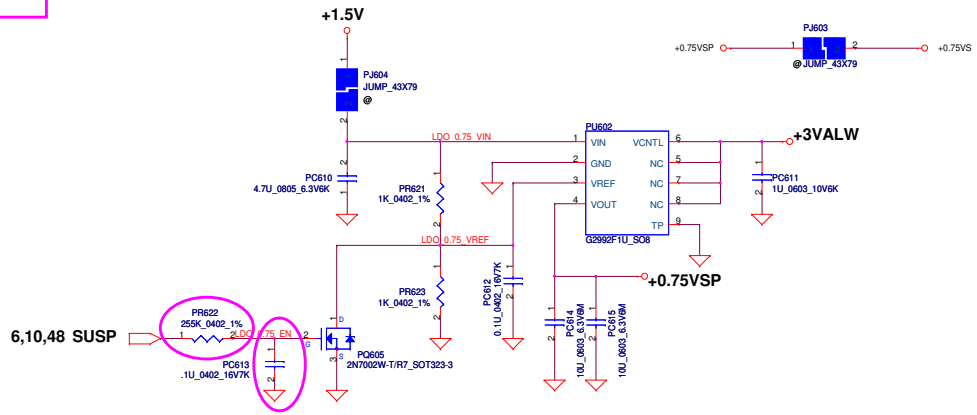


VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR +VCCSAP/+0.75VSP

Size: C | Document Number: PIQY0/Y1 | Rev: 1.0

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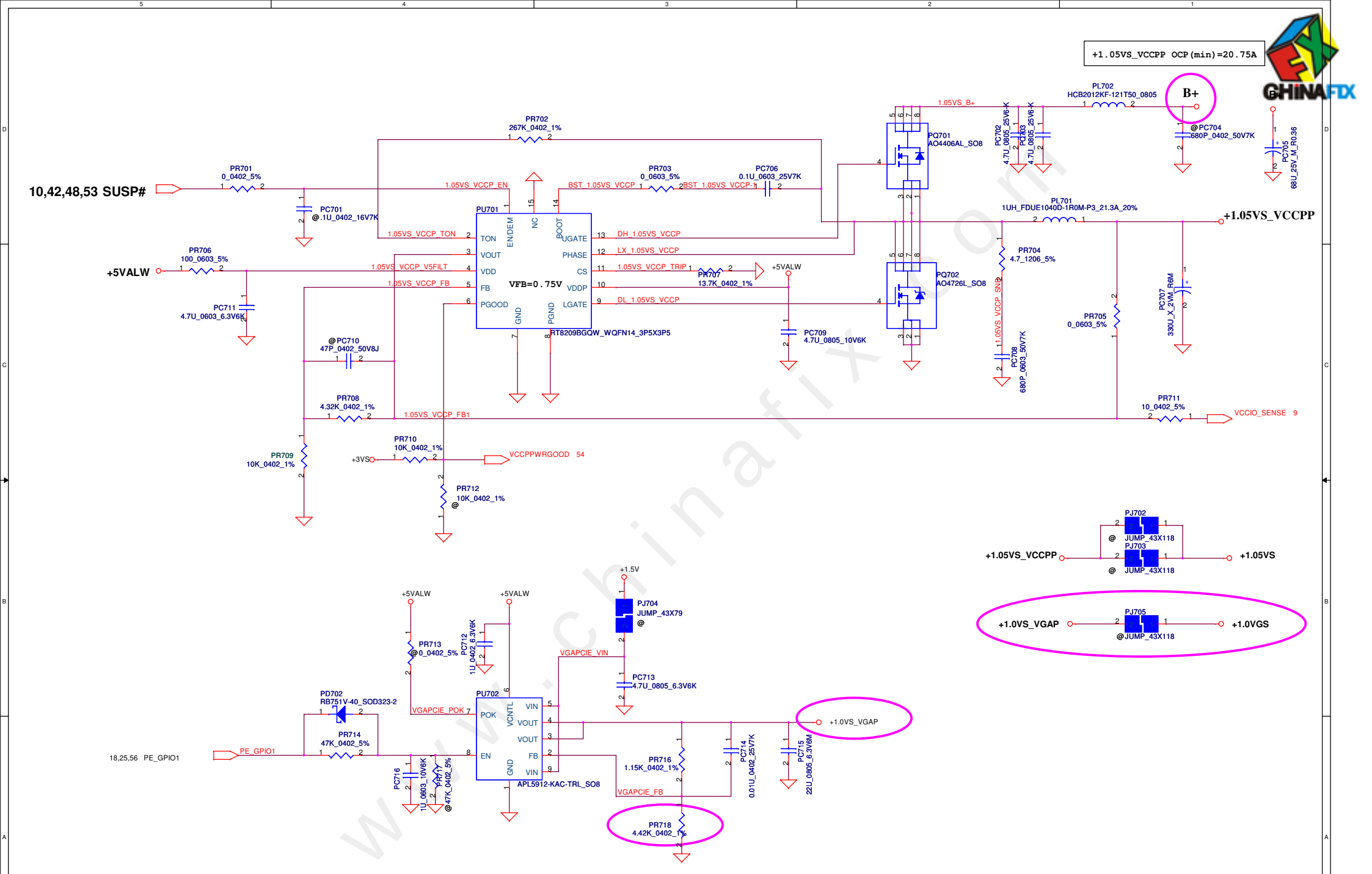

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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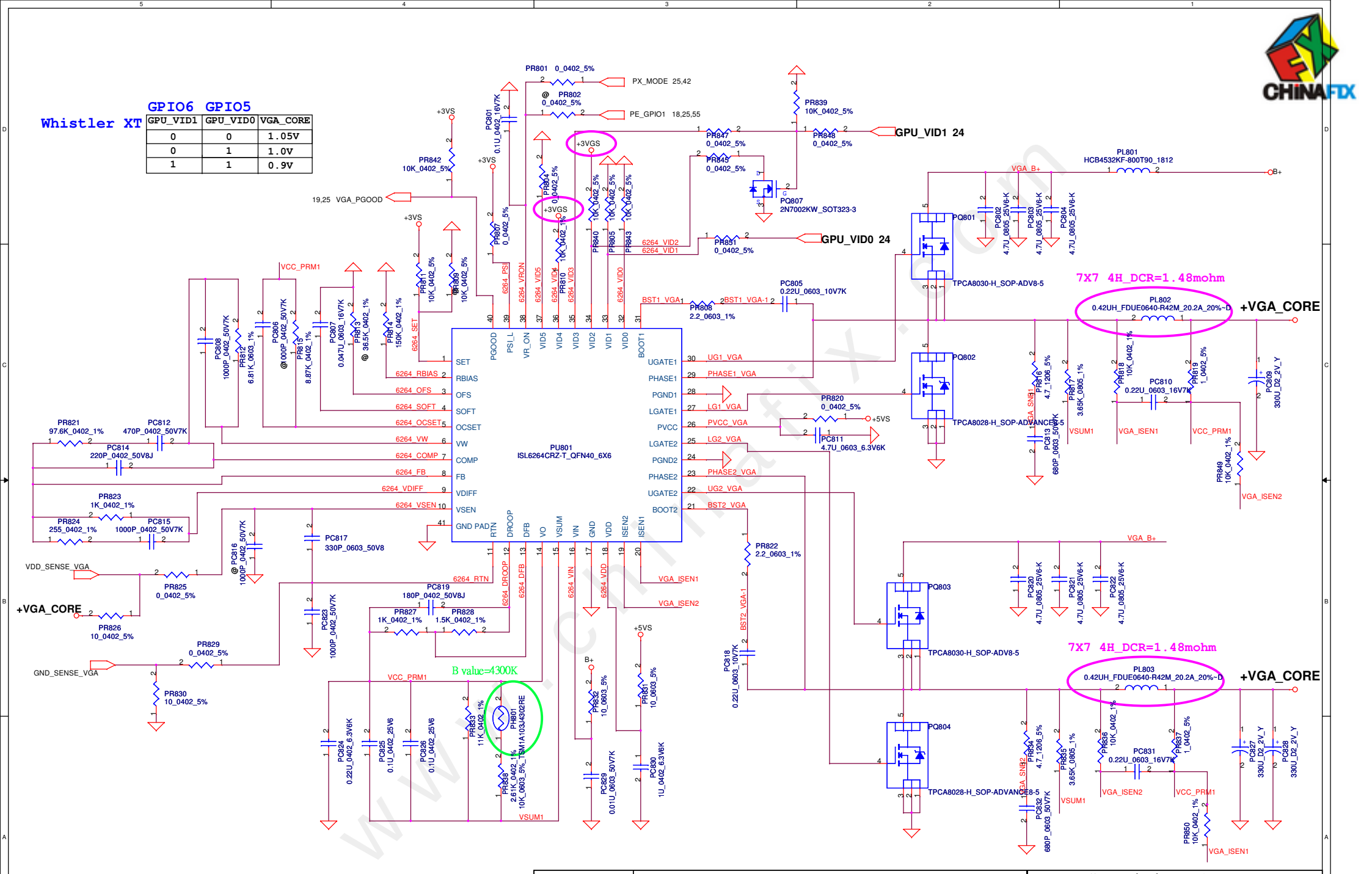
Compal Electronics, Inc.

Title: *PWR +1.05VS_VCCPP/1.0VS_VGA*

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 55 of 63



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Compal Electronics, Inc.

Title: Power-VGA_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, May 11, 2011 | Sheet 56 of 63

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Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

PU901 ISL95831CRZ-T_TQFN48_6X6

PU902 ISL6208CRZ-T_QFN8

PR936
QC:19.1K
DC:19.6K

PR956
QC:3.724K
DC:2.15K

PR959
QC:1.54K=120A
DC:887=70A

QC: PC935
DC: PC933

PR943
0 ohm =>98A (Vboot=0v)
590 ohm=>91A (Vboot=0v)

B value=4700K

B value=4700K

B value=4250K

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Disable Pre-charge		PR102, PR103, PR104, PR107, PD102, PD104, PQ102, PQ103, PQ104		
2	Back to Back MOS change		PQ301, PQ302, PQ303		
3	Battery Learning function		PQ205		
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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QIQY2 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				SDV
1		P23	Change U8 to SA00004R500	Customer need to change
2		P23	Del C998/ C1067/ C343/ C339/ C382/ C376/ C377/ R692	For VGA function
3		P23	Change Q69 to Q75, Q68 to Q76, U56 to U62, U60 to U64, Q87 to Q109, Q86 to Q110, C732 to C777, U59 to U66, R872 to R890, U37 to U41	For VGA function
4		P42	Del R994/ R999/ D46/ Q91	For EC function
5		P15	Del PJP2/ R67/ R257/ R261	For PCH function
6		P23	Del C386/ C732/ R1400/ R1360	For VGA function
7		P33	Del R354/ R3461/ R1372/ R1373 Del R185/ R434/ Q84/ R1022/ Q92/ CV253~CV260/ Q115/R1144/ R1143/ L67/ R997/ R1321	For HDMI function
8		P44	BT_OFF# change to BT_ON#	For BT function
9		P35	EC_PME# change to LAN_WAKE#	For LAN wake funcion
10		P32	CMOS_OFF# change to CMOS_ON#	For CMOS function
11		P45	U11 from SB000007010 change to SB548000210	For +1.5VGS function
12		P32	D31~D35 from +5VS change to +CRT_VCC_CONN	For CRT function
13		P15	U4 from SA00004EEJ0 change to SA00004EEV0	PCH from rev.B2 change to rev.B3
14		P14	R133 from 0 ohm change to 33 ohm	For BIOS ROM function
				SIT
1		P23	Add C69 22Uf_0805 cap for +BIF_VDDC.	For vendor feedback
2		P23	Reserve R613 & R614 to pull up +3VS.	For VGA function
3		P23	Change 0 ohm to R_short --- R10/R1002/R1014/R1029/R109/ R11/R1111/R1114/R1116/R1280/R1281/R1282/R1283/R1285/ R130/R1320/R1336/R1342/R1323/R14/R181R19/R190/R193/R196/ R198/R207/R22/R222/R254R256/R258/R26/R260/R263/R265/R269 /R270/R272R273/R274/R276/R277/R278/R281/R282/R283/R284/ R285/R286/R288/R289/R293/R295/R302/R303/R313/R40/R432/ R52/R53/R668/R710/R824/R825/R880/R882/R885/R886/R891/ R922/R941/R969/R973/R993/R996.	For IO/ PCH/ VGA function
4		P45	U39/ U62 /U44 from SA000039E00 change to SA00003TV00.	For USB function
5		P18	Del net name PCH_GPIO51 connect to RP1 pin2.	For VGA function
6		P25	C351 from 0.1uF_0603 change to 0.047uF_0402.	For VGA function
7		P10	ADD PJP2 jump.	For PCH function
8		P43	U41 from SA000031C00 change to SA00001TC00.	For LID function
9		P25	R352 from 0 ohm change to 330K ohm.	For VGA function
10		P25	Add C343 & C346 for reserve.	For VGA function
11		P25	Q121 from SBX01240010 change to SB000008J10.	For VGA function

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Issued Date	2010/11/30	Deciphered Date	2009/01/06

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Title: PIR (HW)

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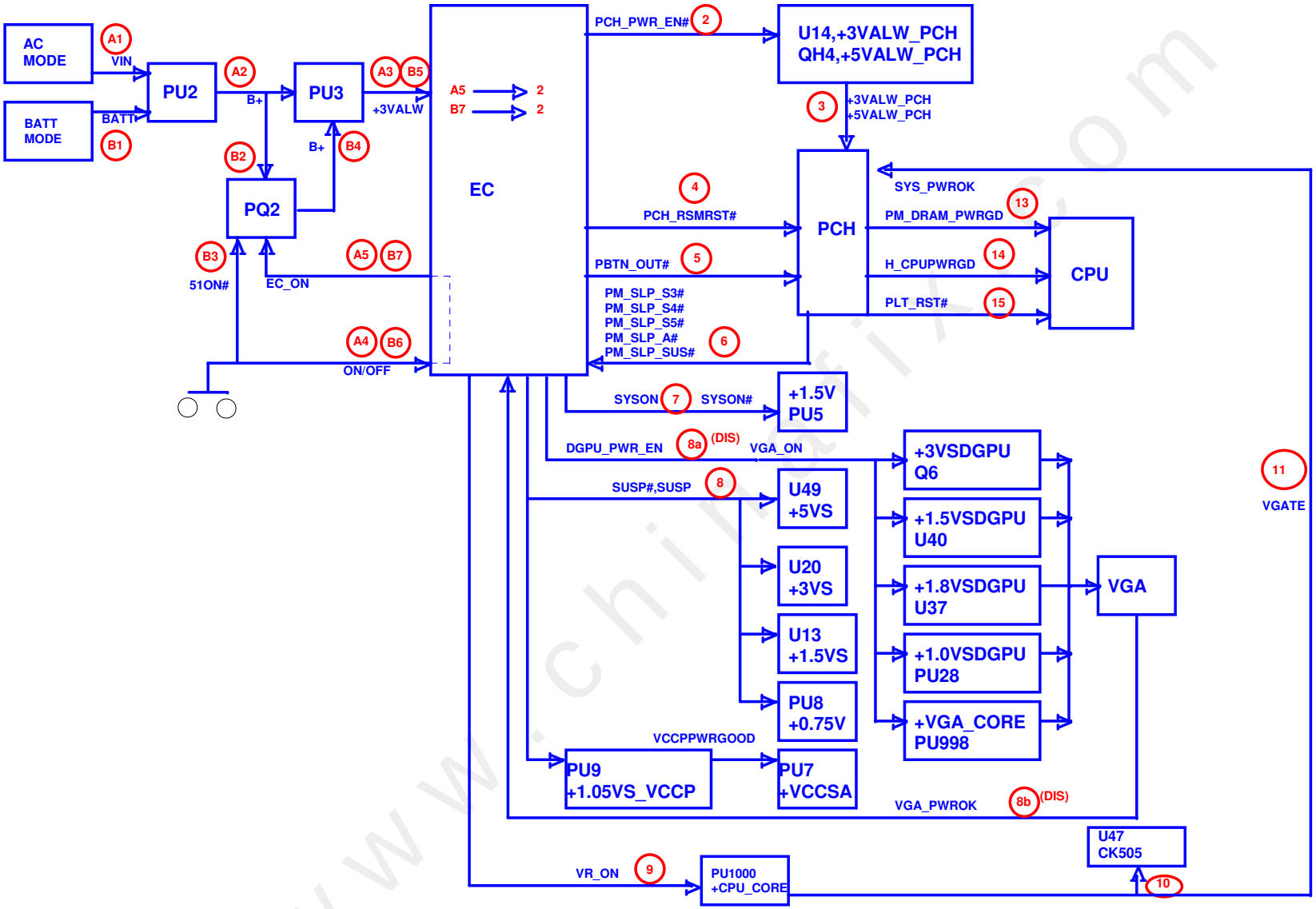

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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title: Power sequence
				Size: Custom; Document Number: QIQY2 LA6884P; Rev: 1.0
				Date: Wednesday, May 11, 2011; Sheet 60 of 63

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