

# JE40 HR

## DIS/UMA/Muxless Schematics Document

### Sandy Bridge

### Intel PCH

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

HR UMA

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Title

**Cover Page**

Size  
A3

Document Number

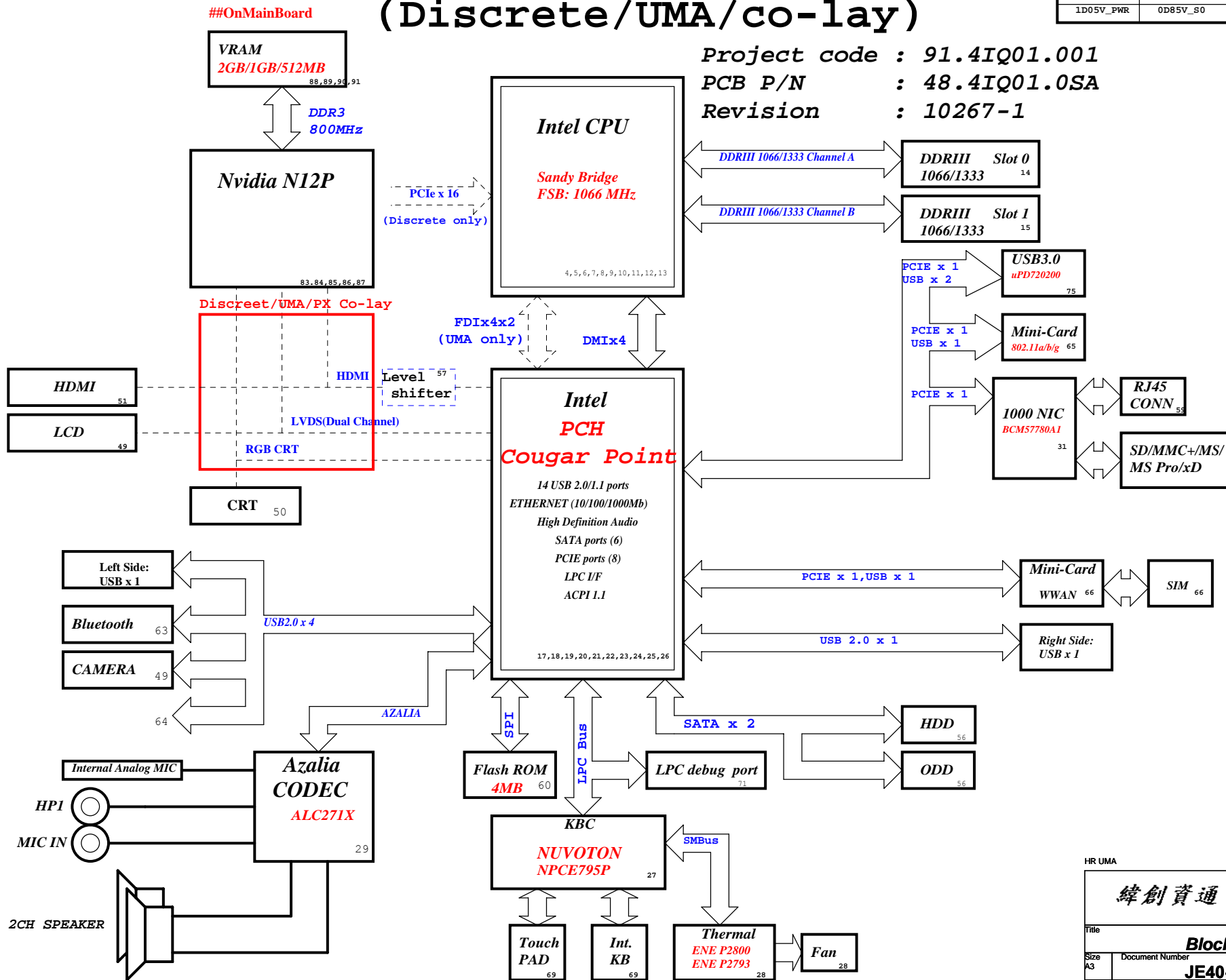
**JE40-HR**

Rev  
**-1**

Date: Thursday, December 02, 2010

Sheet 1 of 102

# JE40 HR Block Diagram (Discrete/UMA/co-lay)



Project code : 91.4IQ01.001  
PCB P/N : 48.4IQ01.0SA  
Revision : 10267-1

SYSTEM DC/DC APL5916KAI 48		CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHRD 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title <b>Block Diagram</b>		
Size A3	Document Number <b>JE40-HR</b>	Rev <b>-1</b>
Date: Thursday, December 02, 2010	Sheet 2 of 102	

PCH Strapping Huron River Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. <b>Disable Danbury:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Processor Strapping Huron River Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I2 C / SMBus Addresses		Ref Des	HURON RIVER ORB	
Device		Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Table of Content

JE40-HR

Rev -1

Date: Thursday, December 02, 2010

Sheet 3 of 102

SSID = CPU

CPU1A  
SANDY  
62.10055.421  
Change:62.10053.611  
2nd = 62.10055.321  
3rd = 62.10040.821

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

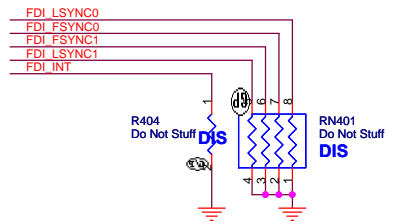
Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Lane reversal does not apply to FDI sideband signals.

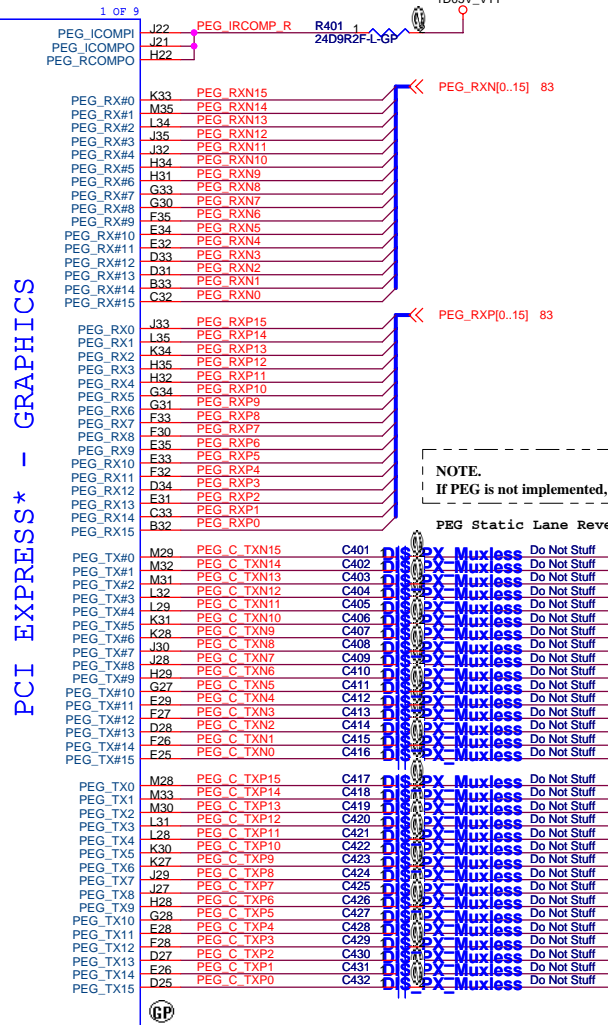
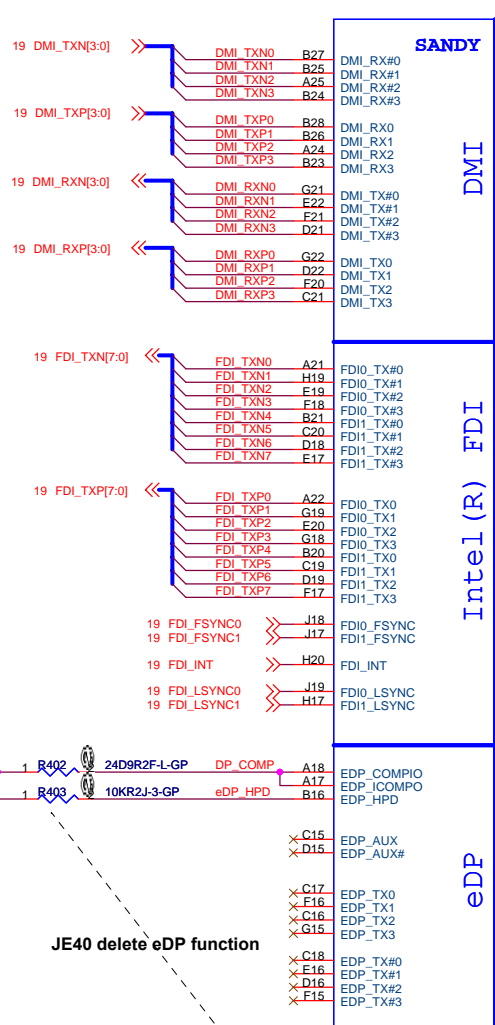
Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.



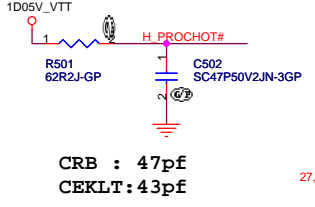
NOTE:  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



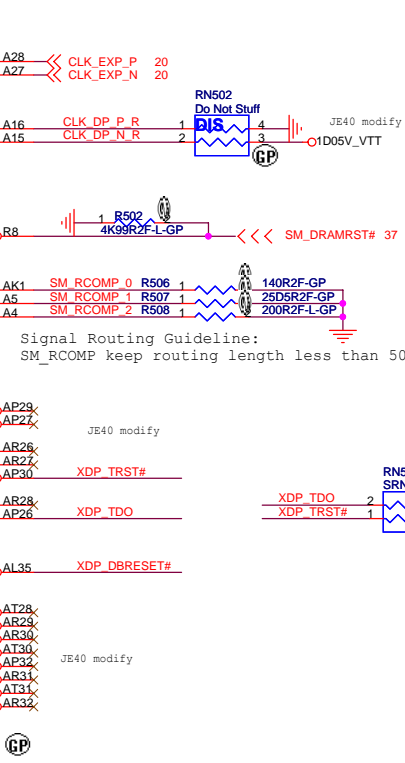
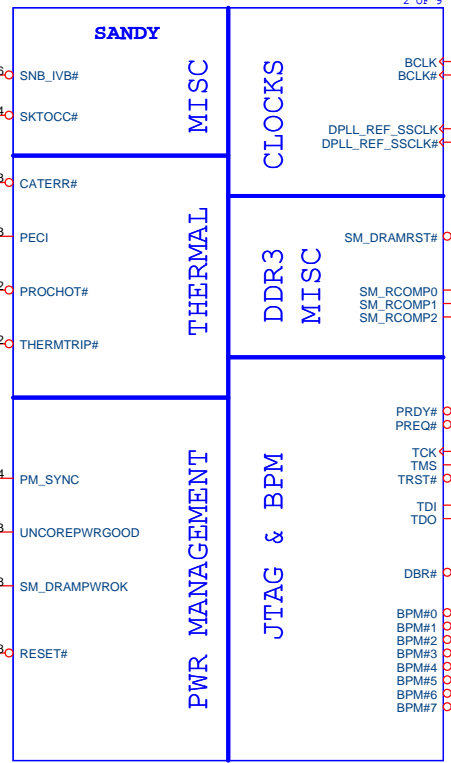
NOTE:  
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal			
PEG_TXN[0..15]	83	PEG_TXN15	Do Not Stuff
PEG_TXN14	Do Not Stuff	PEG_TXN14	Do Not Stuff
PEG_TXN13	Do Not Stuff	PEG_TXN13	Do Not Stuff
PEG_TXN12	Do Not Stuff	PEG_TXN12	Do Not Stuff
PEG_TXN11	Do Not Stuff	PEG_TXN11	Do Not Stuff
PEG_TXN10	Do Not Stuff	PEG_TXN10	Do Not Stuff
PEG_TXN9	Do Not Stuff	PEG_TXN9	Do Not Stuff
PEG_TXN8	Do Not Stuff	PEG_TXN8	Do Not Stuff
PEG_TXN7	Do Not Stuff	PEG_TXN7	Do Not Stuff
PEG_TXN6	Do Not Stuff	PEG_TXN6	Do Not Stuff
PEG_TXN5	Do Not Stuff	PEG_TXN5	Do Not Stuff
PEG_TXN4	Do Not Stuff	PEG_TXN4	Do Not Stuff
PEG_TXN3	Do Not Stuff	PEG_TXN3	Do Not Stuff
PEG_TXN2	Do Not Stuff	PEG_TXN2	Do Not Stuff
PEG_TXN1	Do Not Stuff	PEG_TXN1	Do Not Stuff
PEG_TXN0	Do Not Stuff	PEG_TXN0	Do Not Stuff

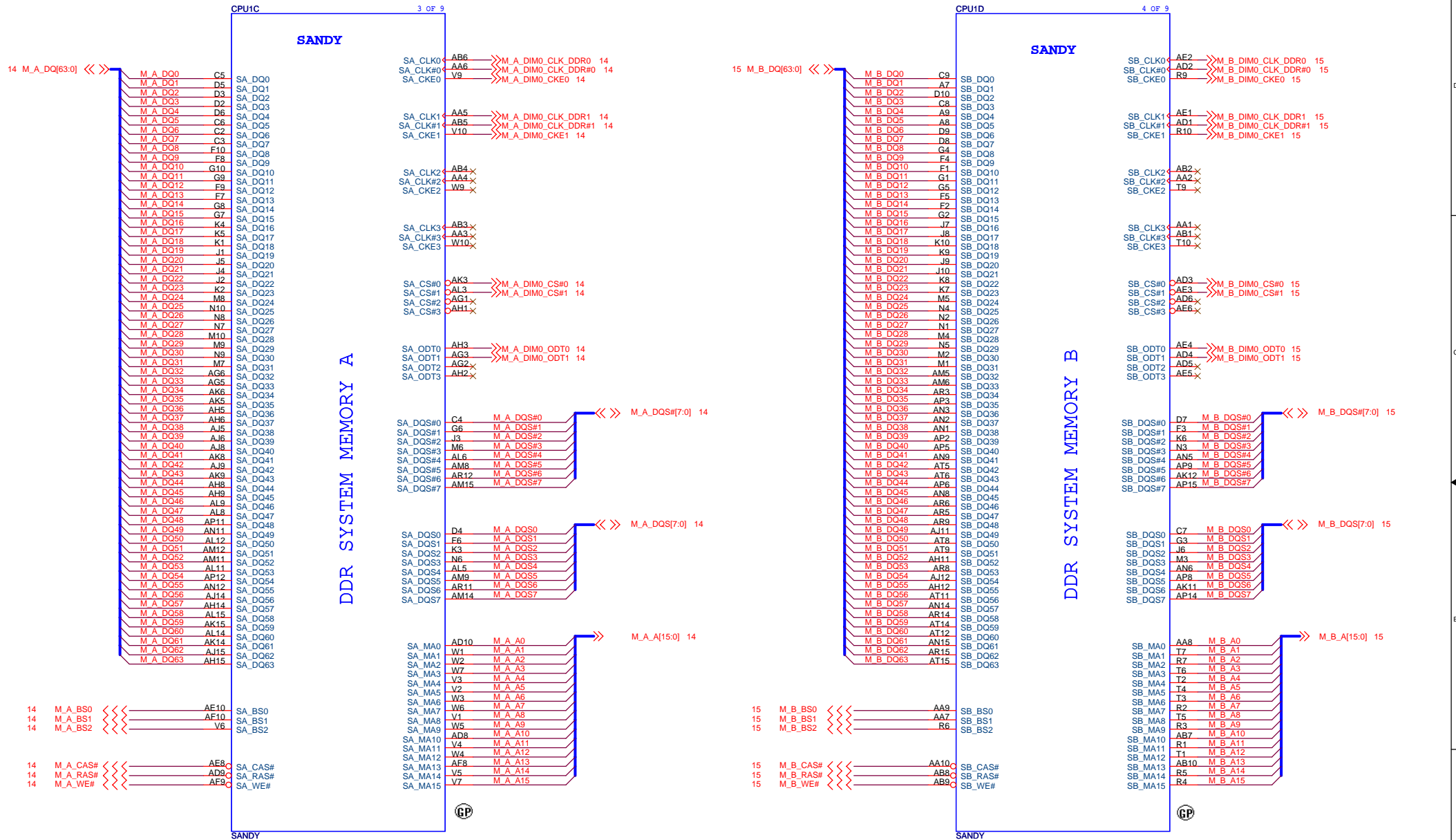
SSID = CPU



Connect EC to PROCHOT# through inverting OD buffer.



SSID = CPU



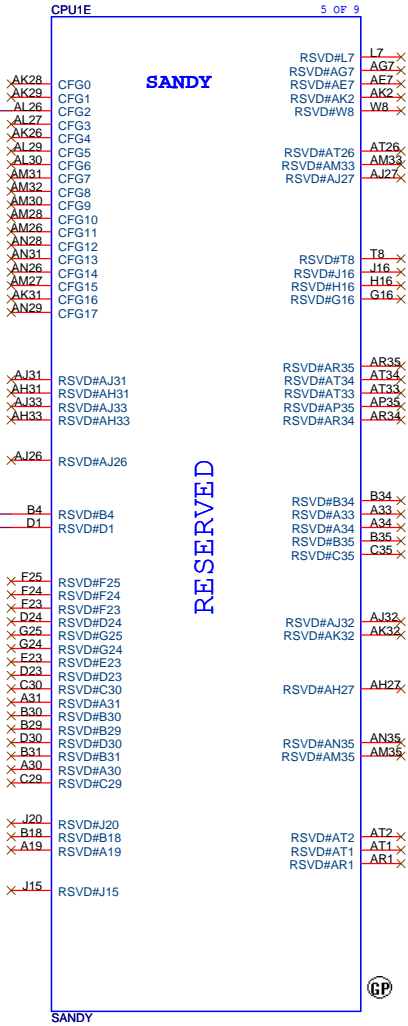
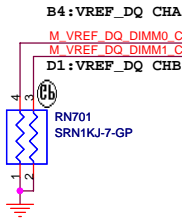
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SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

DIS\_PX\_Muxless

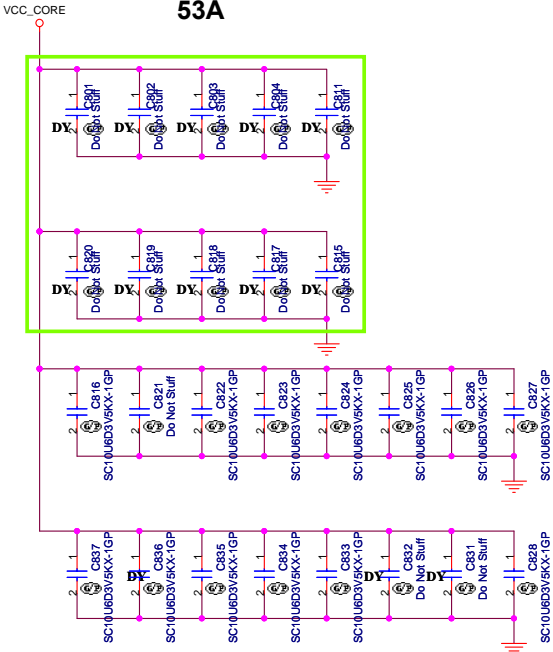


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Title			
CPU (RESERVED)			
Size	Document Number	Rev	
A3	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	7 of 102

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:  
4 x 470 uF at Bottom Socket Edge  
8 x 22 uF at Top Socket Cavity  
8 x 22 uF at Top Socket Edge  
8 x 22 uF at Bottom Socket Cavity

SANDY

VCC\_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AG25 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
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- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

PEG AND DDR

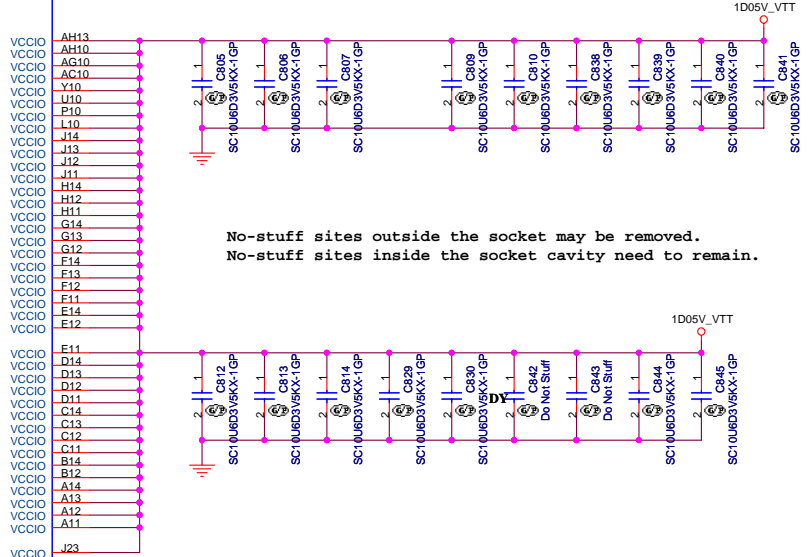
CORE SUPPLY

SVID

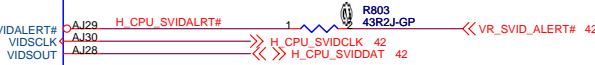
SENSE LINES

- VIDALERT#
- VIDSCLK
- VIDSOUT
- VCC\_SENSE
- VSS\_SENSE
- VCCIO\_SENSE
- VSSIO\_SENSE

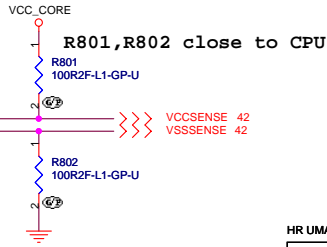
VCCIO Output Decoupling Recommendation:  
2 x 330 uF (3 x 330 uF for 2012 capable designs)  
5 x 22 uF & 5 x 0805 no-stuff at Bottom  
7 x 22 uF & 2 x 0805 no-stuff at Top



No-stuff sites outside the socket may be removed.  
No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7  
For CRB VIDALERT# need to pull high 75 ohm close to CPU



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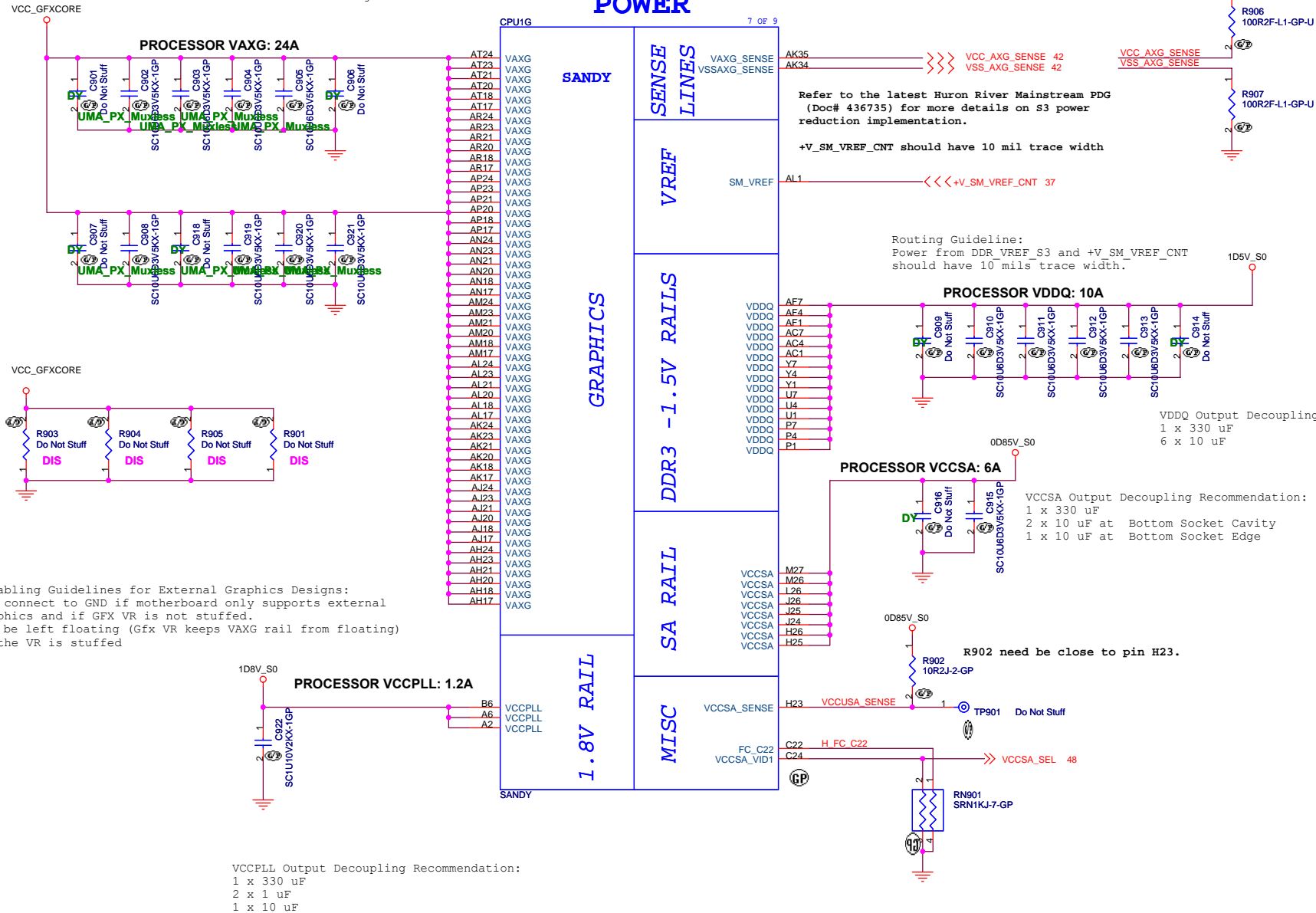
Title			
CPU (VCC_CORE)			
Size	Document Number	Rev	
Custom	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	8 of 102



SSID = CPU

```
VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge
```

R906,R907 close to CPU



Disabling Guidelines for External Graphics Designs:  
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.  
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

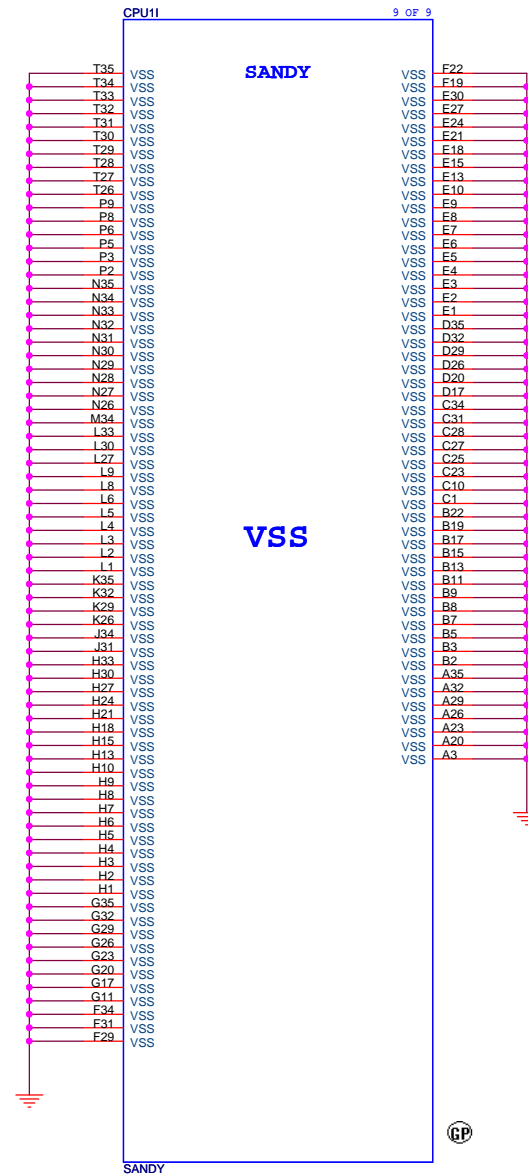
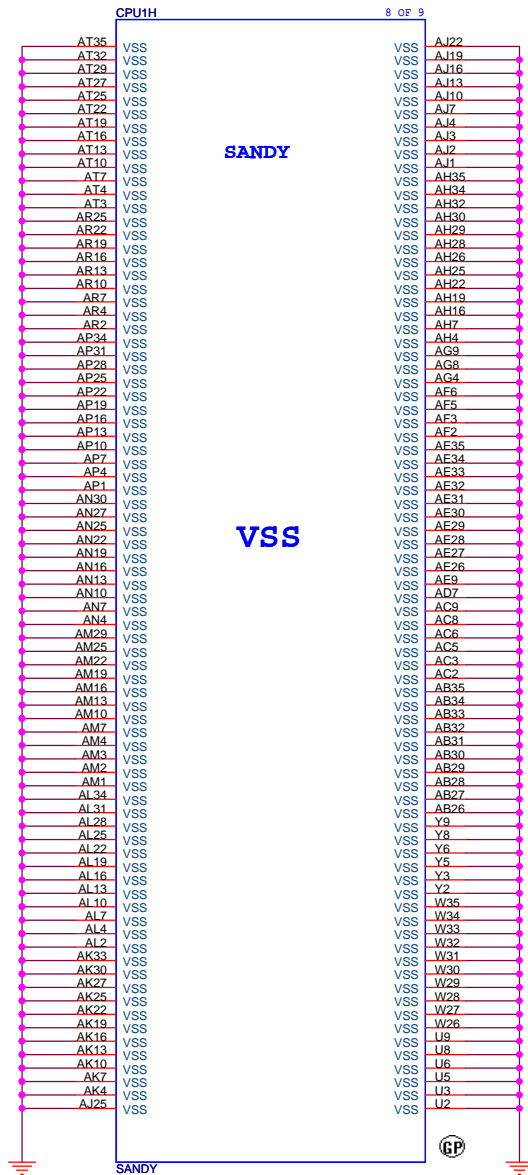
VCCPLL Output Decoupling Recommendation:  
1 x 330 uF  
2 x 1 uF  
1 x 10 uF

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Title			
<b>CPU (VCC GFXCORE)</b>			
Size A3	Document Number		Rev
	<b>JE40-HR</b>		<b>-1</b>
Date:	Thursday, December 02, 2010	Sheet 9 of	102

**SSID = CPU**



5	4	3	2	1
D				
C				
B				
A				
JE40 delete XDP function				
5	4	3	2	1

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Title

Size  
A3

Document Number  
**JE40-HR**

Date: Thursday, December 02, 2010

**SDP**

**Rev**

**-1**

Sheet 11 of 102

(Blanking)

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 12 of 102

5					4					3					2					1				
D																								
C																								
(Blanking)																								
B																								
A																								
HR UMA																	<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>							
Title																	Reserved							
Size A4		Document Number JE40-HR																Rev -1						
Date: Thursday, December 02, 2010																	Sheet		13		of		102	
5					4					3					2					1				

# SSID = MEMORY

<< M\_A\_A[15:0] 6

6 M\_A\_BS2 >>>

6 M\_A\_BS0 >>>

6 M\_A\_BS1 >>>

6 M\_A\_DQ[63:0]

<< M\_A\_DQS#[7:0] 6

<< M\_A\_DQS[7:0] 6

6 M\_A\_DIM0\_ODT0 >>>

6 M\_A\_DIM0\_ODT1 >>>

15,37 DDR3\_DRAMRST# >>>

M\_A A0 98  
M\_A A1 97  
M\_A A2 96  
M\_A A3 95  
M\_A A4 92  
M\_A A5 91  
M\_A A6 90  
M\_A A7 89  
M\_A A8 88  
M\_A A9 85  
M\_A A10 107  
M\_A A11 84  
M\_A A12 83  
M\_A A13 113  
M\_A A14 80  
M\_A A15 78  
A16/BA2 79

M\_A DQ0 5  
M\_A DQ1 7  
M\_A DQ2 15  
M\_A DQ3 17  
M\_A DQ4 4  
M\_A DQ5 16  
M\_A DQ6 16  
M\_A DQ7 18  
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M\_A DQ44 146  
M\_A DQ45 148  
M\_A DQ46 158  
M\_A DQ47 160  
M\_A DQ48 163  
M\_A DQ49 165  
M\_A DQ50 175  
M\_A DQ51 177  
M\_A DQ52 164  
M\_A DQ53 166  
M\_A DQ54 174  
M\_A DQ55 176  
M\_A DQ56 181  
M\_A DQ57 183  
M\_A DQ58 191  
M\_A DQ59 193  
M\_A DQ60 180  
M\_A DQ61 182  
M\_A DQ62 192  
M\_A DQ63 194

M\_A DQS#0 10  
M\_A DQS#1 27  
M\_A DQS#2 45  
M\_A DQS#3 62  
M\_A DQS#4 135  
M\_A DQS#5 152  
M\_A DQS#6 169  
M\_A DQS#7 186  
DQS#0# 10  
DQS#1# 27  
DQS#2# 45  
DQS#3# 62  
DQS#4# 135  
DQS#5# 152  
DQS#6# 169  
DQS#7# 186

M\_A DQ50 12  
M\_A DQ51 29  
M\_A DQ52 47  
M\_A DQ53 64  
M\_A DQ54 137  
M\_A DQ55 154  
M\_A DQ56 171  
M\_A DQ57 188  
DQ50# 12  
DQ51# 29  
DQ52# 47  
DQ53# 64  
DQ54# 137  
DQ55# 154  
DQ56# 171  
DQ57# 188

DDR\_VREF\_S3 126  
VREF\_CA 1  
VREF\_DQ 30  
RESET# 30  
VTT1 203  
VTT2 204

H=4mm

NP1 NP2  
RAS# 110  
WE# 113  
CAS# 115  
CS0# 114  
CS1# 121  
CKE0 73  
CKE1 74  
CK0 101  
CK0# 103  
CK1 102  
CK1# 104  
DM0 11  
DM1 28  
DM2 46  
DM3 63  
DM4 136  
DM5 153  
DM6 170  
DM7 187  
SDA 200  
SCL 202  
EVENT# 198  
VDDSPD 199  
SA0 197  
SA1 201  
NC#1 77  
NC#2 122  
NC#/TEST 125  
VDD1 75  
VDD2 76  
VDD3 81  
VDD4 82  
VDD5 87  
VDD6 88  
VDD7 93  
VDD8 94  
VDD9 99  
VDD10 100  
VDD11 105  
VDD12 106  
VDD13 111  
VDD14 112  
VDD15 117  
VDD16 118  
VDD17 123  
VDD18 124  
VSS 2  
VSS 3  
VSS 8  
VSS 9  
VSS 13  
VSS 14  
VSS 19  
VSS 20  
VSS 25  
VSS 26  
VSS 31  
VSS 32  
VSS 37  
VSS 38  
VSS 43  
VSS 44  
VSS 48  
VSS 49  
VSS 54  
VSS 55  
VSS 60  
VSS 61  
VSS 65  
VSS 66  
VSS 71  
VSS 72  
VSS 127  
VSS 128  
VSS 133  
VSS 134  
VSS 138  
VSS 139  
VSS 144  
VSS 145  
VSS 150  
VSS 151  
VSS 155  
VSS 156  
VSS 161  
VSS 162  
VSS 167  
VSS 168  
VSS 172  
VSS 173  
VSS 178  
VSS 179  
VSS 184  
VSS 185  
VSS 189  
VSS 190  
VSS 195  
VSS 196  
VSS 205  
VSS 206

DM1  
DDR3-204P-122-GP  
62.10017.251  
2nd = 62.10017.V51  
3rd = 62.10017.M51  
4th = 62.10017.X41

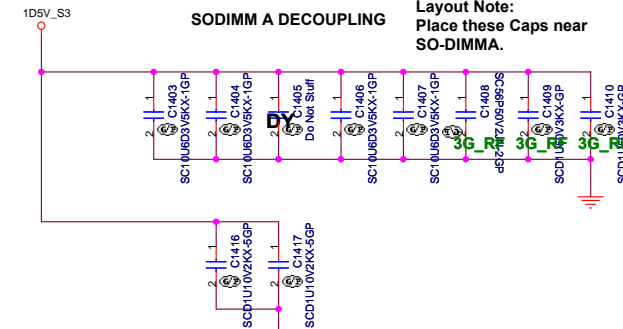
## Thermal EVENT

TS#\_DIMM0\_1 R1403 10KR2J-3-GP

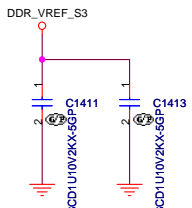
Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

## SODIMM A DECOUPLING

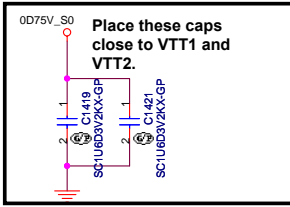
Layout Note:  
Place these Caps near  
SO-DIMMA.



PART NUMBER	Height	TYPE



-2



HR UMA

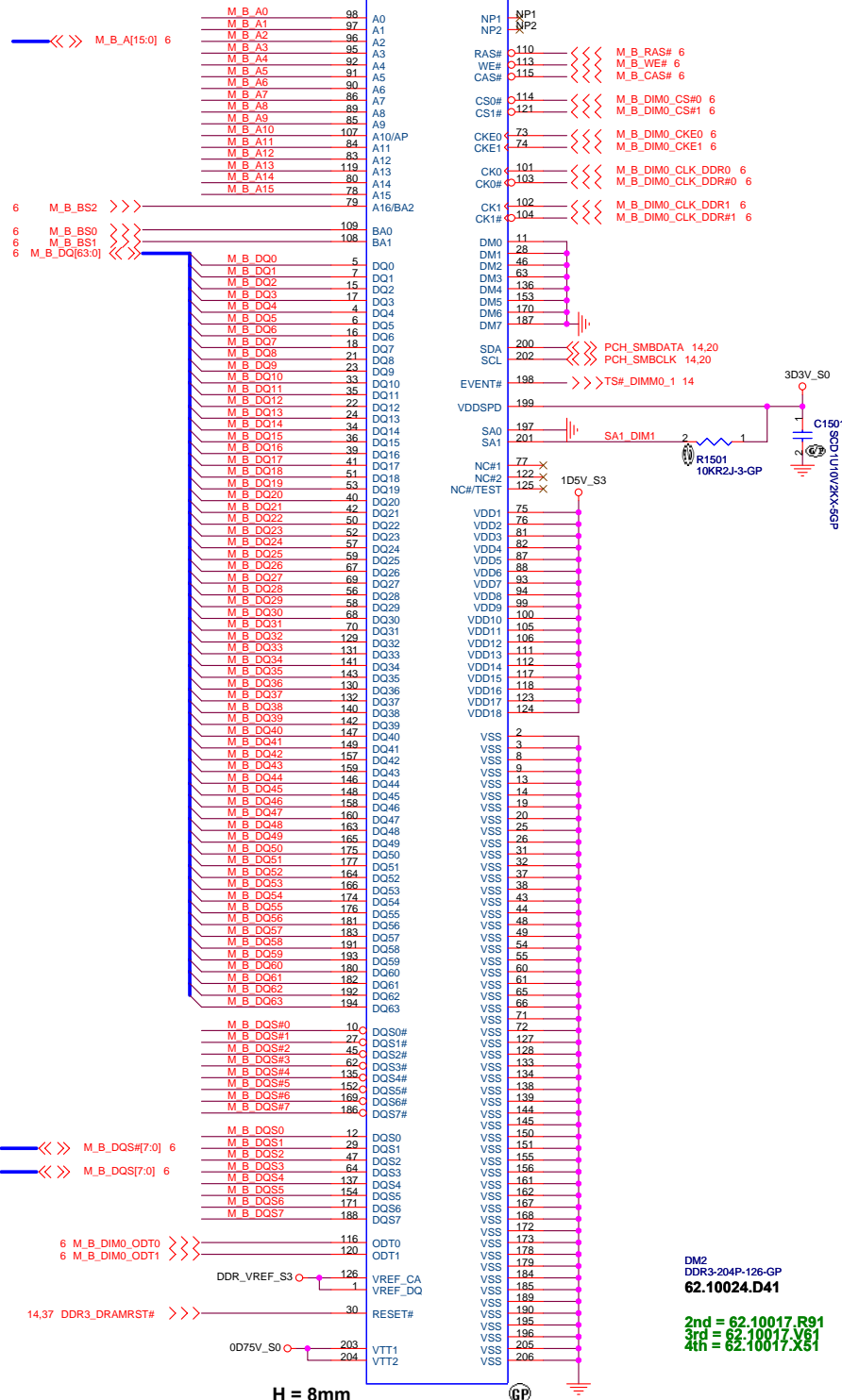
**緯創資通 Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **DDR3-SODIMM1**

Size Custom Document Number **JE40-HR** Rev **-1**

Date: Thursday, December 02, 2010 Sheet 14 of 102

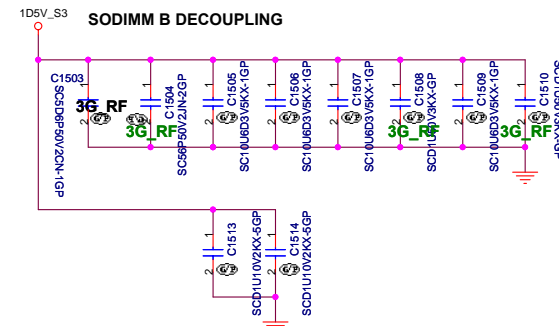
# SSID = MEMORY



Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

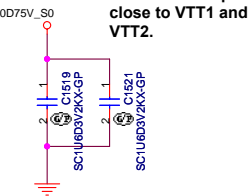
SO-DIMMB is placed farther from  
the Processor than SO-DIMMA

Layout Note:  
Place these Caps near  
SO-DIMMB.



-2

Place these caps  
close to VTT1 and  
VTT2.



H = 8mm

DM2  
DDR3-204P-126-GP  
62.10024.D41

2nd = 62.10017.R91  
3rd = 62.10017.V61  
4th = 62.10017.X51

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

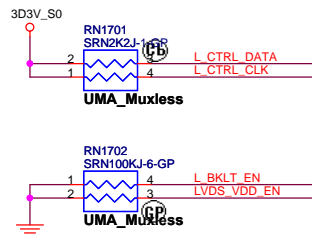
Title			DDR3-SODIMM2		
Size	Custom	Document Number	JE40-HR		
Date:	Thursday, December 02, 2010	Sheet	15	of	102
Rev			-1		

(Blanking)

HR UMA

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Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 16 of 102





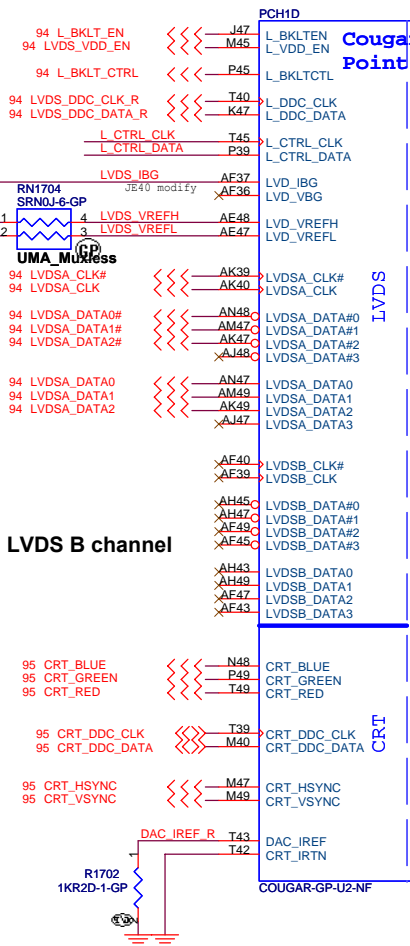
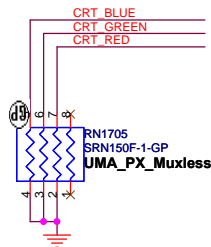
**L\_DDC\_DATA(PAGE17):**  
This signal is on the LVDS interface.  
This signal needs to be left NC if eDP is  
used for the local flat panel display

Place near PCH  
UMA\_Muxless

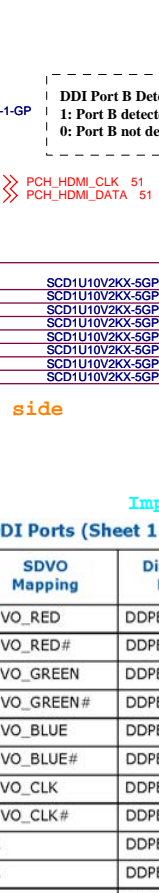
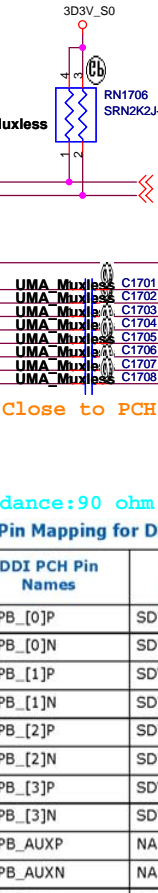
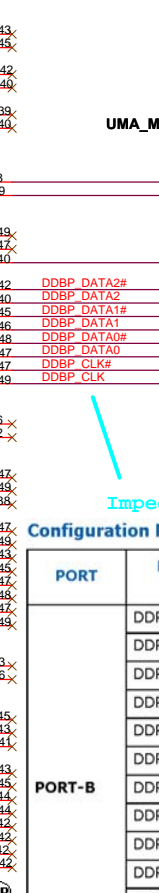
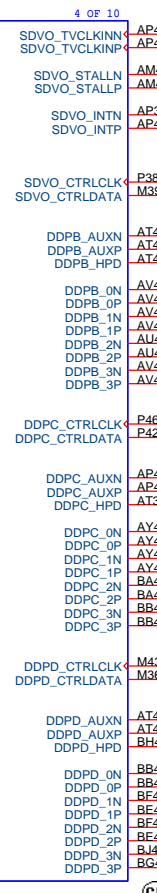
Impedance:90 ohm

JE40 delete LVDS B channel

Close to PCH side



Digital Display Interface

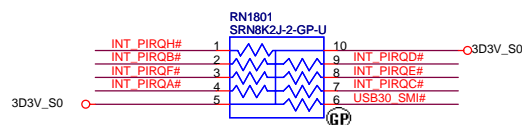


Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

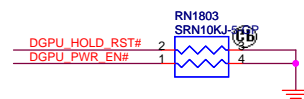
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMIIB_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA

HR UMA

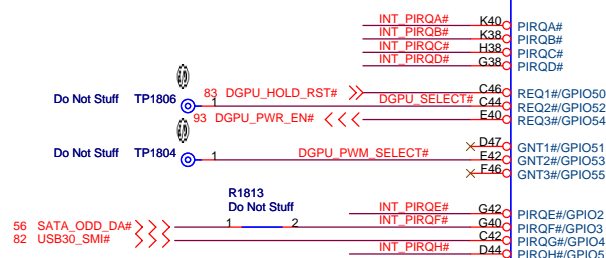
**SSID = PCH**



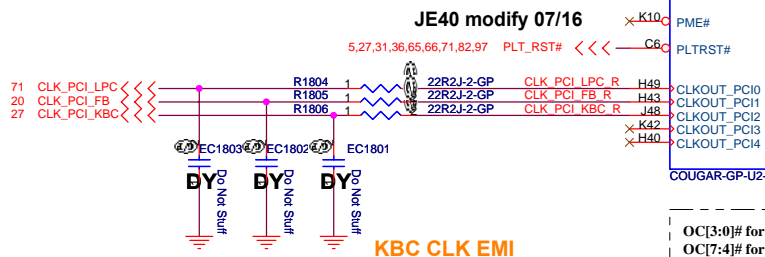
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

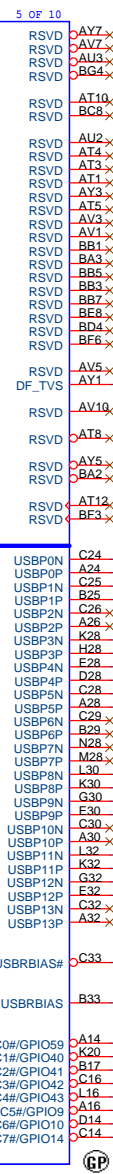
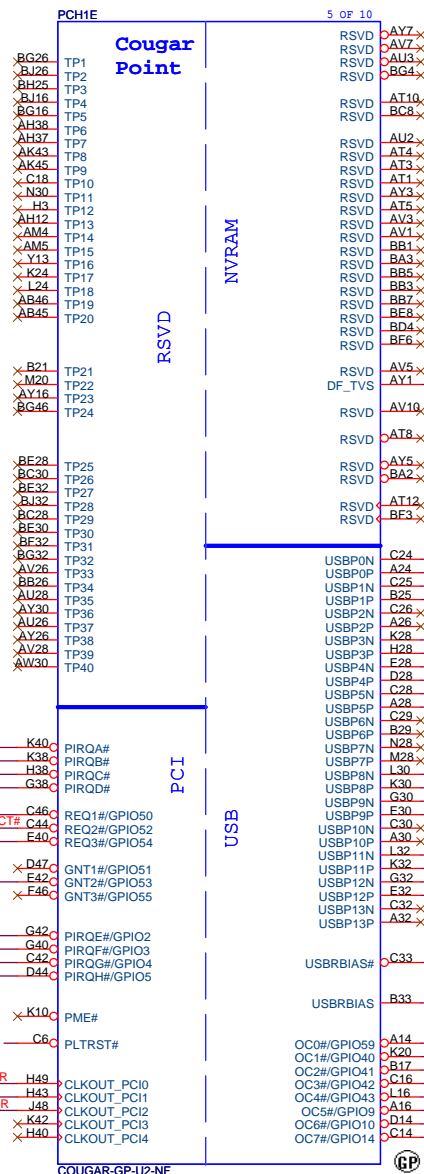


**JE40 modify 07/16**



KBC CLK EMI

OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)

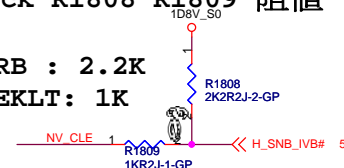


DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K

CEKLT: 1K



2 ~~X~~ USB Ext. port 1 (HS)

```

* External debug port use on Huron river platform

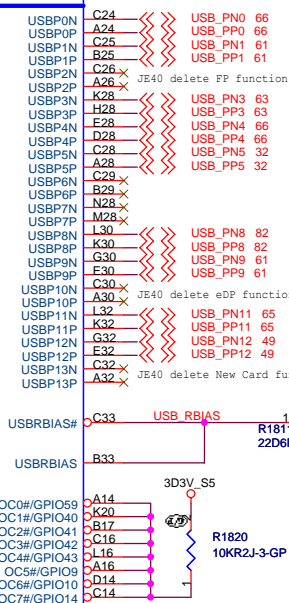
```

## USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB C
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

**SB add USB port 5**

**JE40 co-lay USB2.0**



### USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**PCH (PCI/USB/NVRAM)**

Size

Document Number

# JE40-HR

Date \_\_\_\_\_

Thursday, December 02, 2010

Sheet 18 of 102

-1

SSID = PCH

4 DMI\_RXN[3:0] <<<>>> 4  
4 DMI\_RXP[3:0] <<<>>> 4  
4 DMI\_TXN[3:0] <<<>>> 4  
4 DMI\_TXP[3:0] <<<>>> 4

FDI\_TXN[7:0] 4  
FDI\_TXP[7:0] 4

Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and  
routing length less than 500  
mils.  
DMI\_IRCOMP keep W=4 mils and  
routing length less than 500  
mils.

Deep S4/S5 Supported

Deep S4/S5 Not Supported

VccDSW3\_3

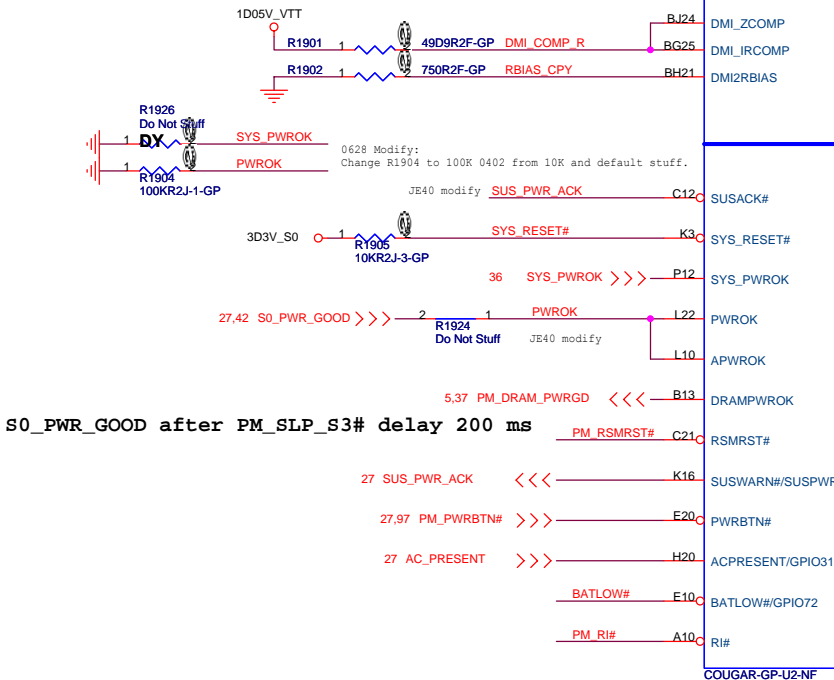
DPWROK

VccSUS3\_3

RSMRST#

For platforms not supporting Deep S4/S5

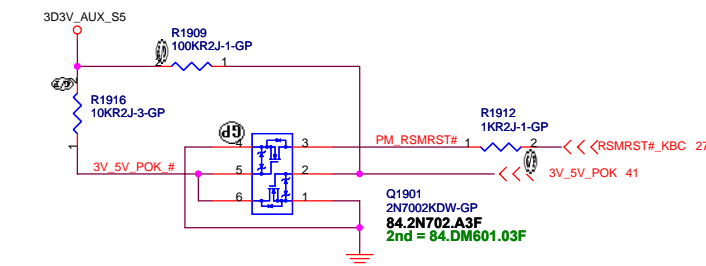
- 1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP\_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30



S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms

PWRBTN#  
This signal has an internal pull-up resistor

PM\_RSMRST#  
CRB : PL 10K  
ANNIE : PL 100K



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

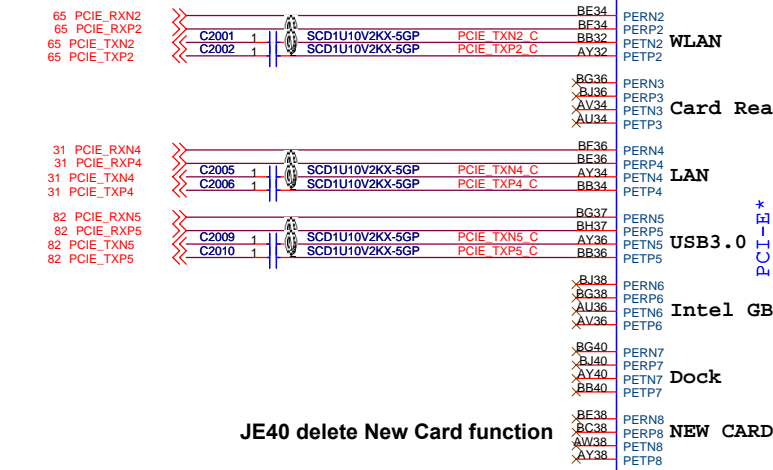
SB modify

HR UMA

緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title PCH (DM I/FDI/PM)  
Size A3 Document Number JE40-HR  
Date: Thursday, December 02, 2010 Sheet 19 of 102  
Rev -1

**SSID = PCH**



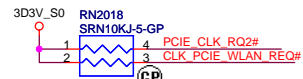
## JE40 delete New Card function

WWAN CLK

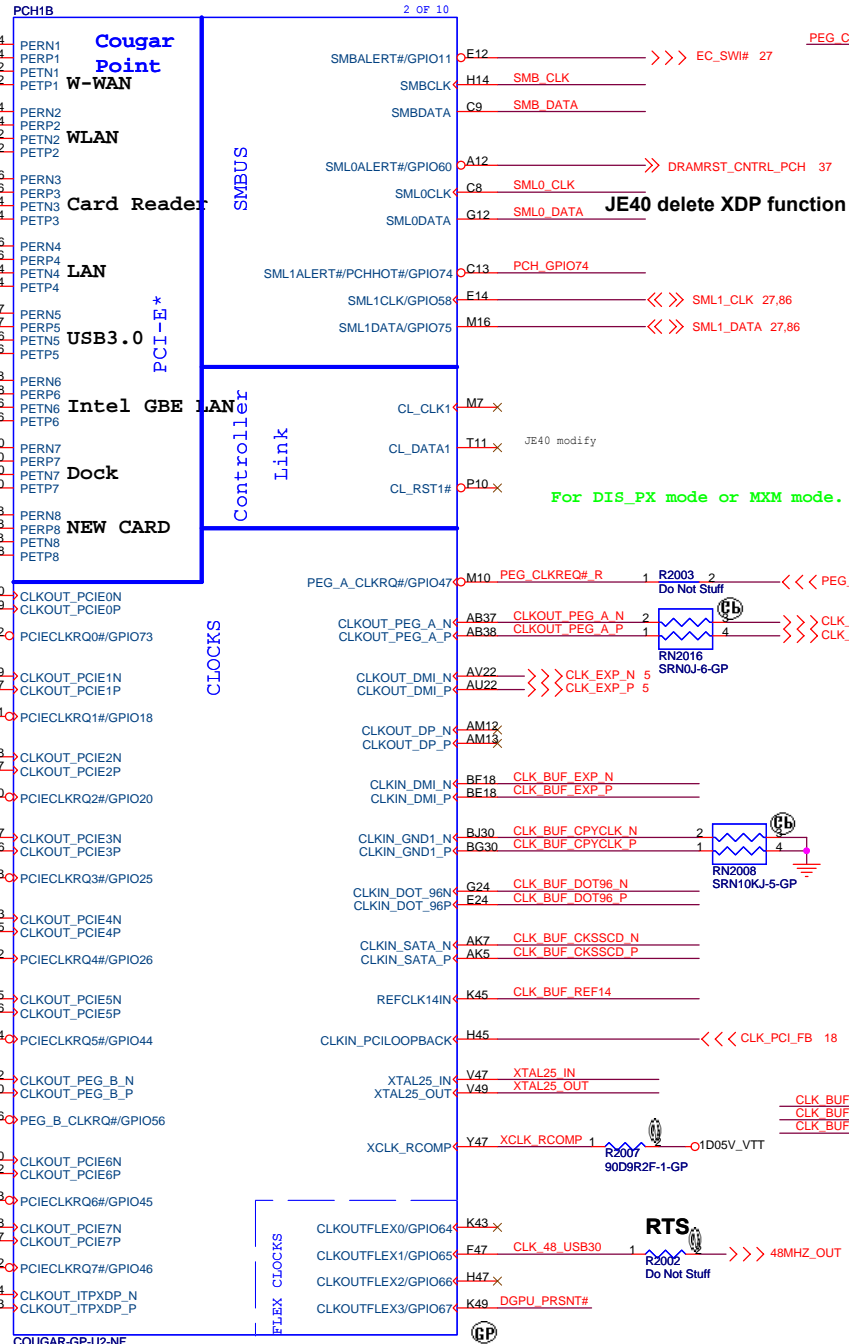
WLAN CLK

LAN CLK

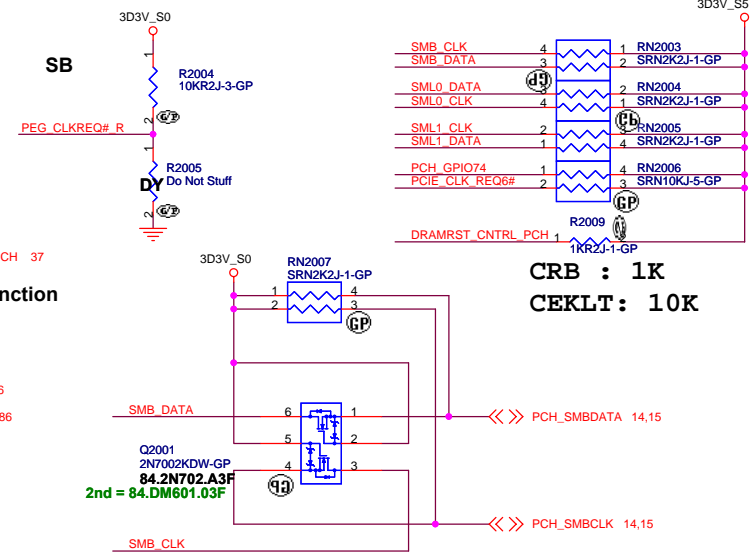
USB3.0 CLK



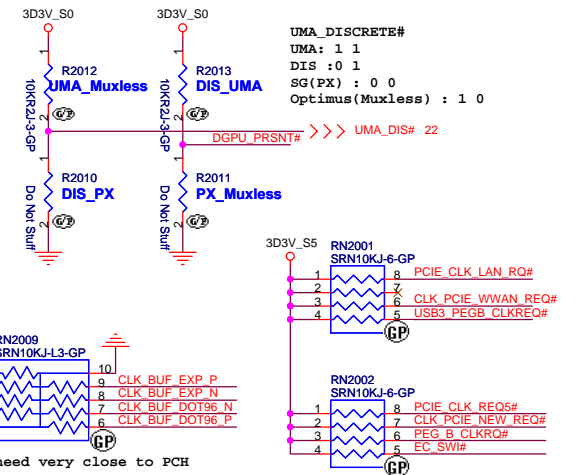
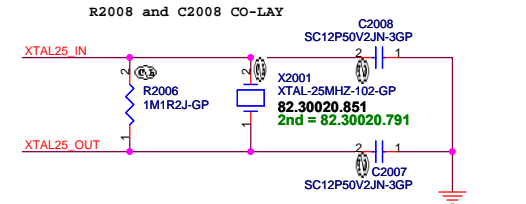
PCIECLKRQ1# and PCIECLKRQ2#  
Support S0 power only



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.



CRB : 1K  
CEKLT: 10K

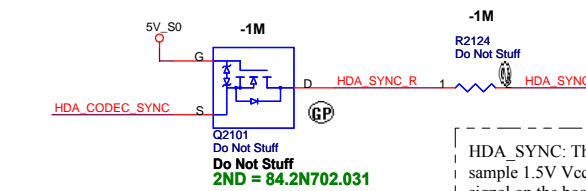
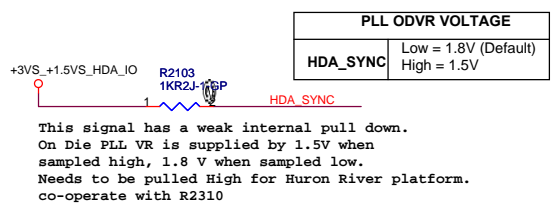
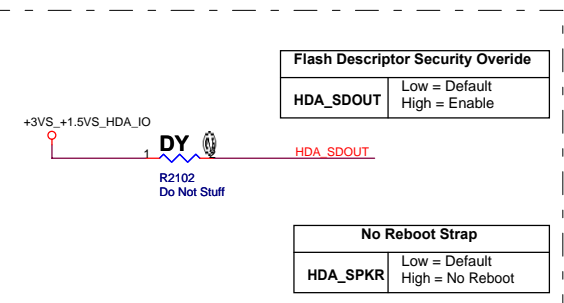
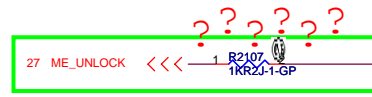
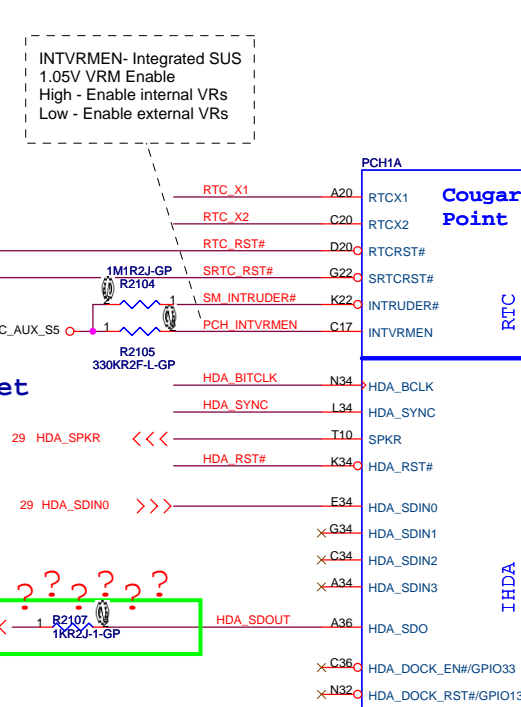
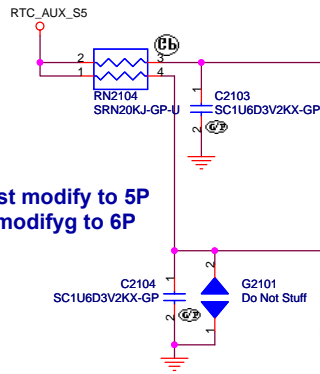
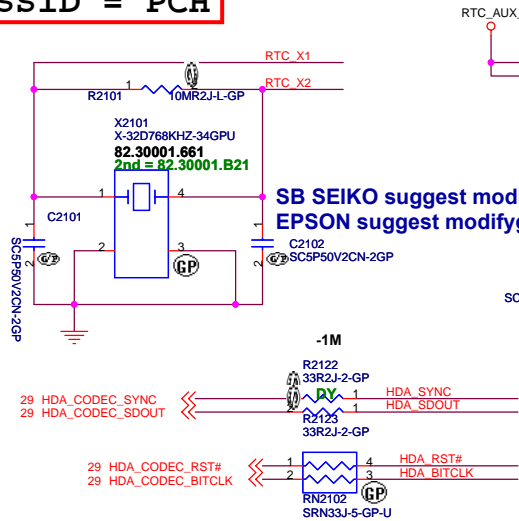


HR UMA

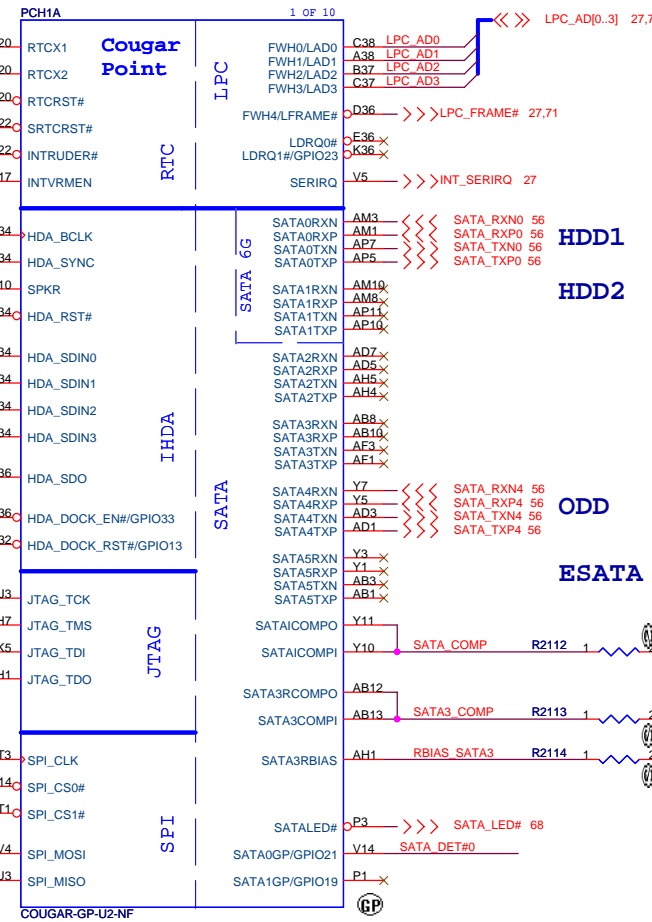
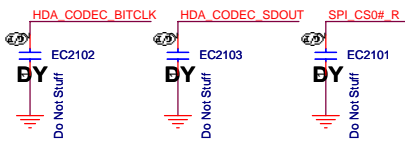
**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>PCH (PCI-E/SMBUS/CLOCK/CL)</b>			
Size A3	Document Number		Rev
	<b>JE40-HR</b>		<b>-1</b>
Date:	Thursday, December 02, 2010	Sheet 20 of	102

SSID = PCH



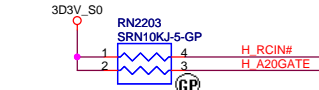
HDA\_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.



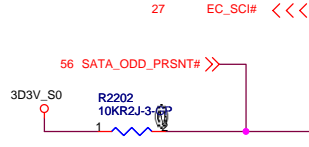
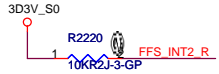


# SSID = PCH

Note:  
For PCH debug with XDP, need to NO STUFF R2218



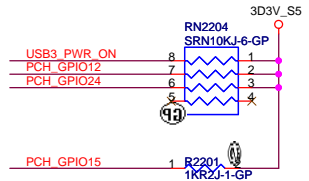
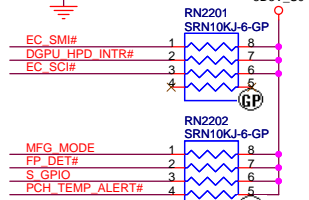
GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.



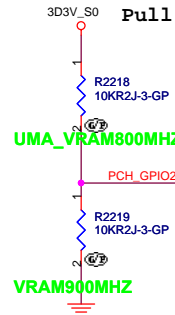
0806 delete TP2202, TP2203  
Do Not Stuff TP2202  
Do Not Stuff TP2203

21 PSW\_CLR# <<<  
JE40 delete FP function

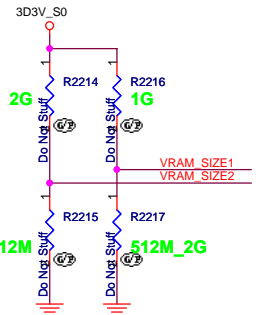
## Pass Word Clear



SB VRAM Frequency  
Pull high: 800MHZ  
Pull low :900MHZ

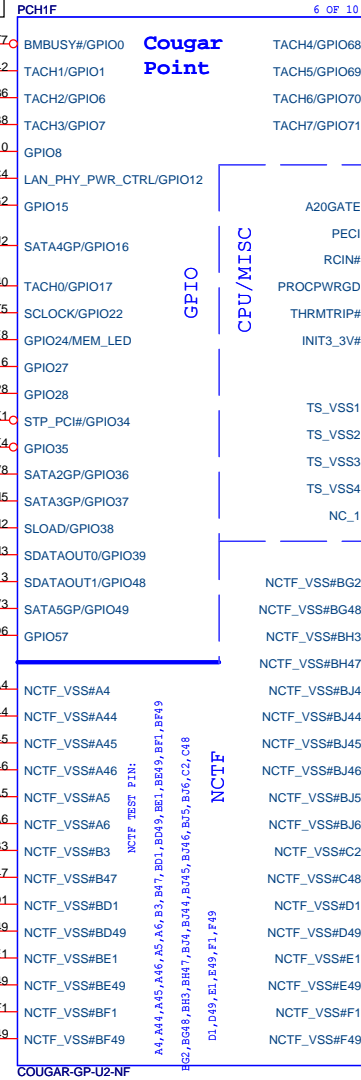


## VRAM Size

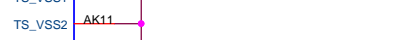
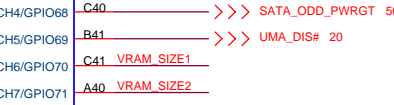


PLL ON DIE VR ENABLE

NOTE:This signal has a weak internal pull-up 20K  
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT  
DISABLED -- LOW (R2212 STUFFED)



## SB add Zero ODD function



SB 公板 check different , check need modify or not  
check intel , R2204

TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They should  
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

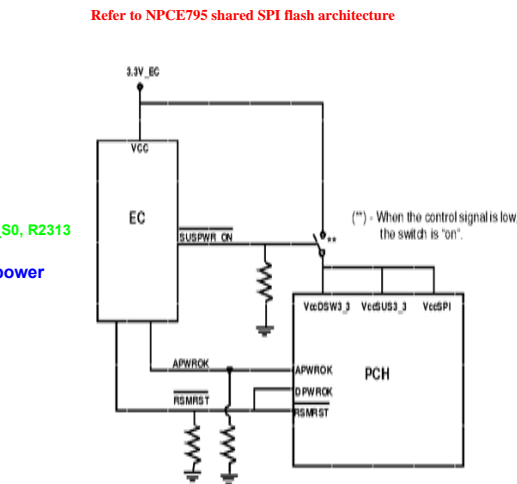
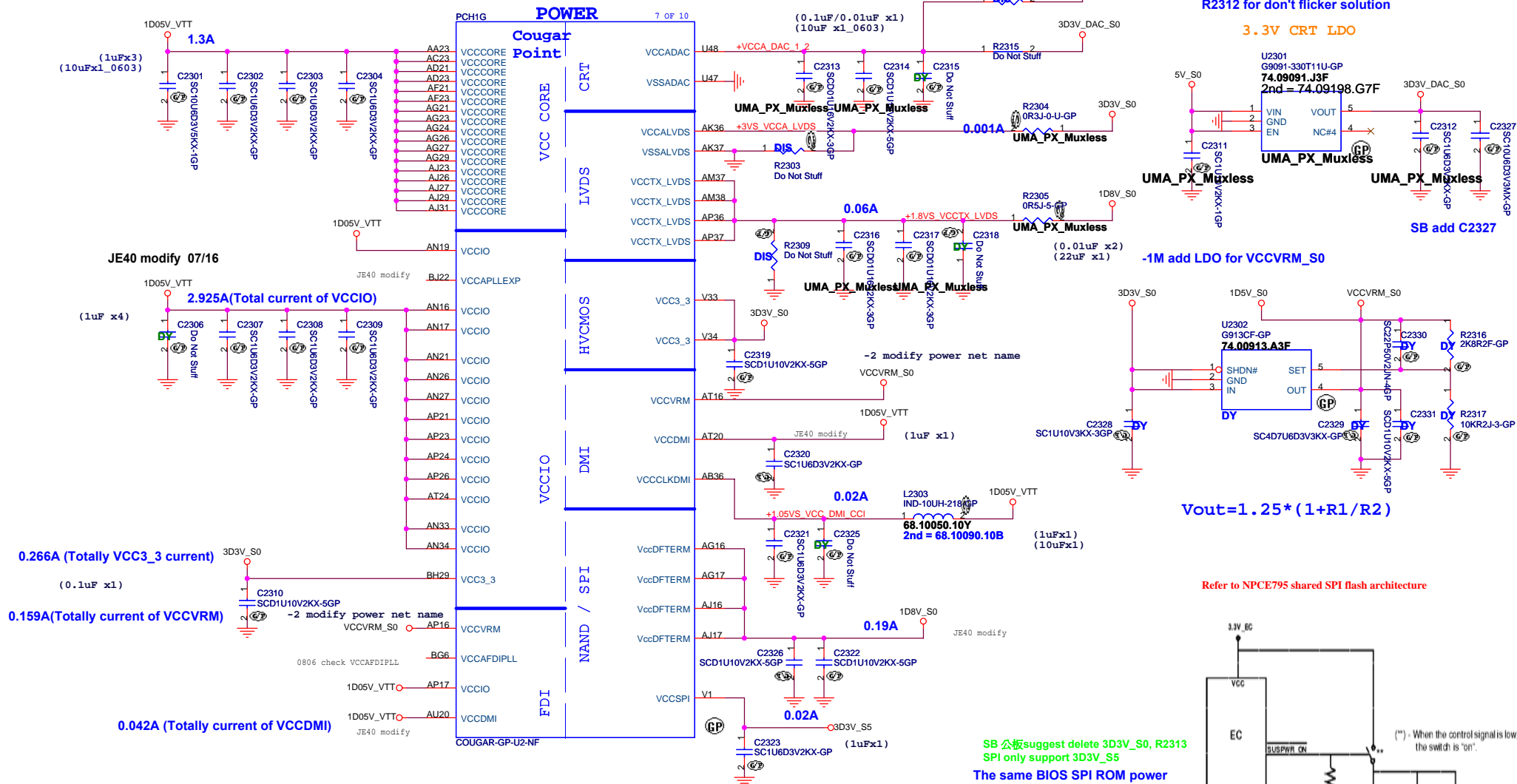
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

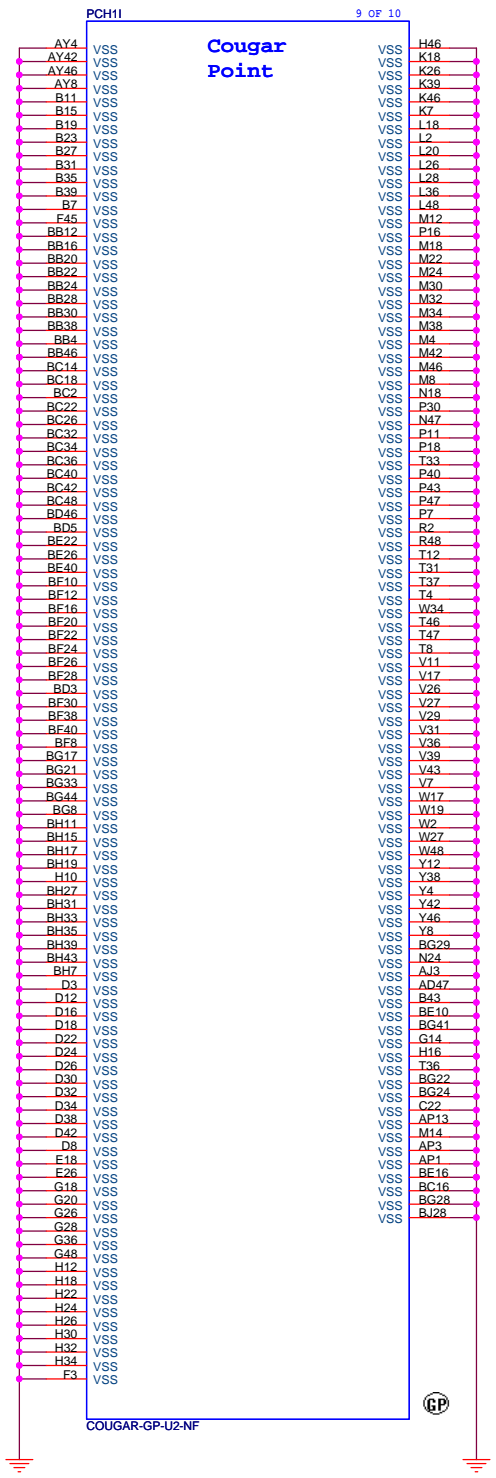
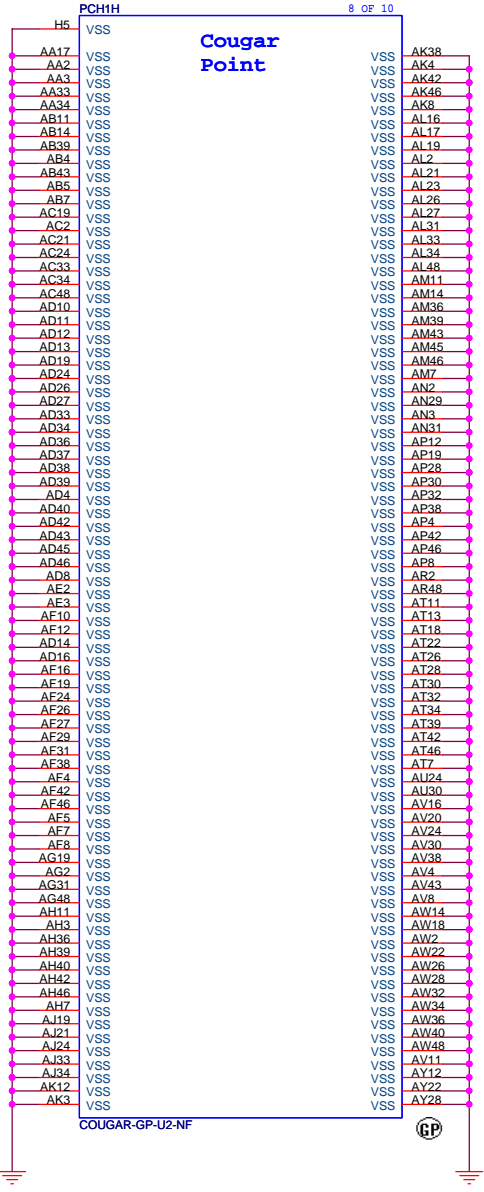
Title		
PCH (GPIO/CPU)		
Size	Document Number	Rev
A3	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 22 of 102

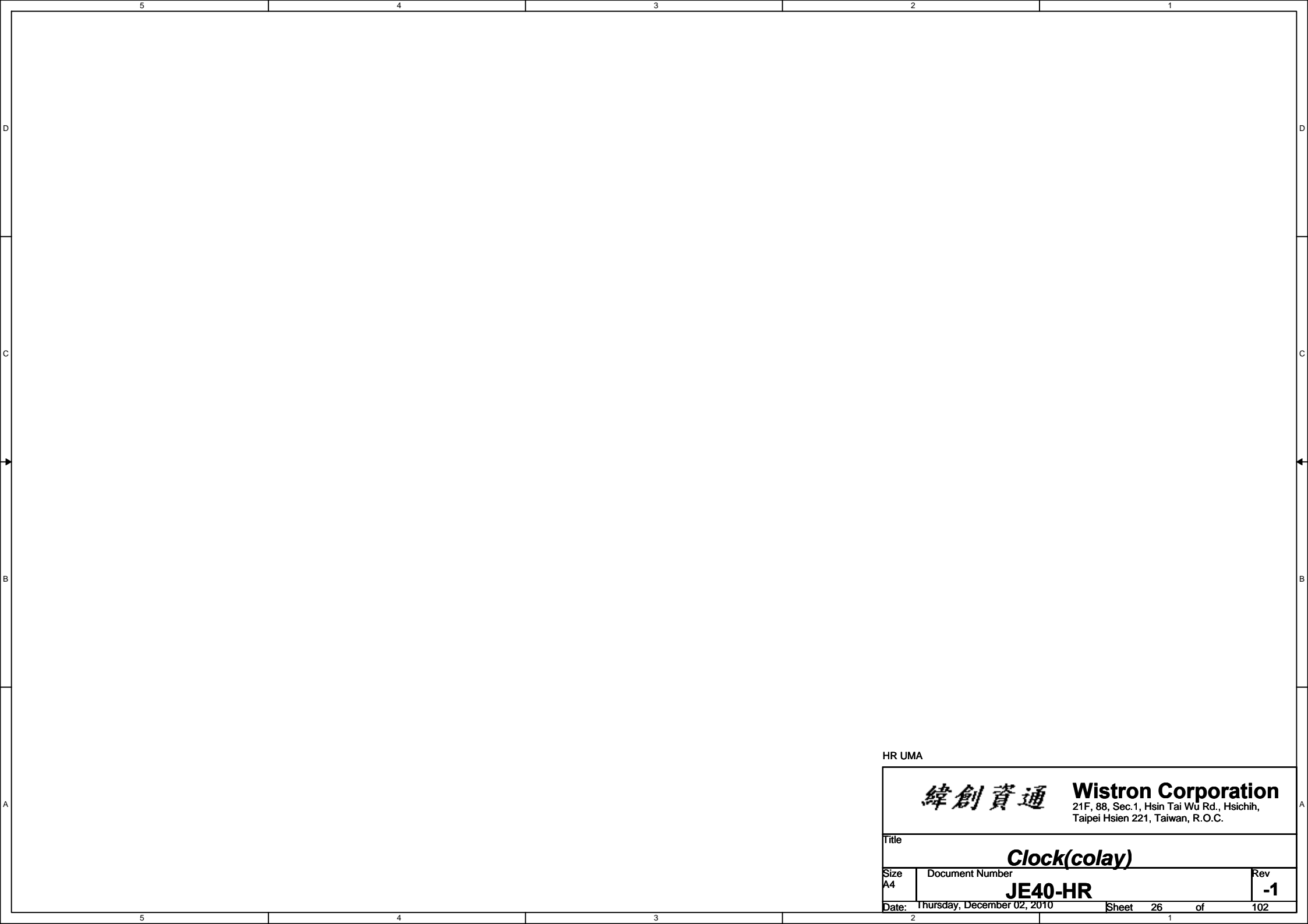






SSID = PCH





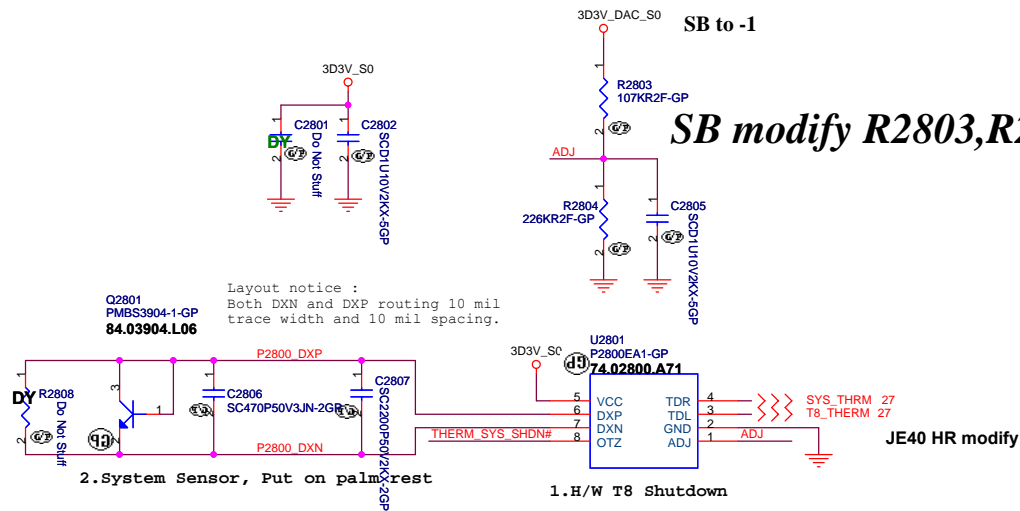
HR UMA

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Title <div>Clock(colay)</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 26 of 102



SSID = Thermal

## Thermal sensor P2800



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

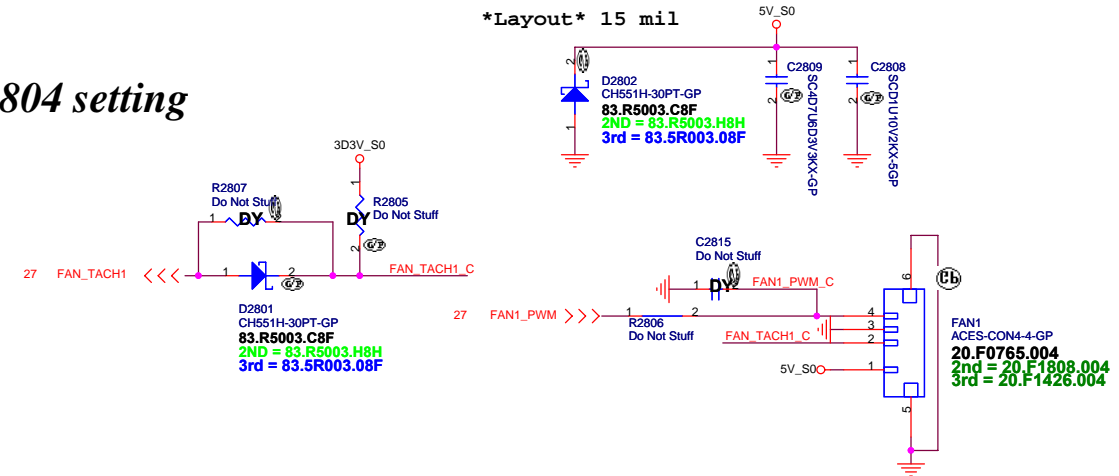
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

## VGA Thermal sensor P2800

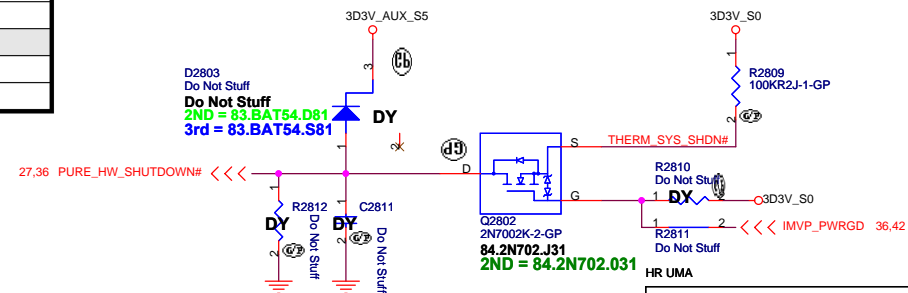
SMBUS modify to Page 84

## Fan controller P2793

\*Layout\* 15 mil

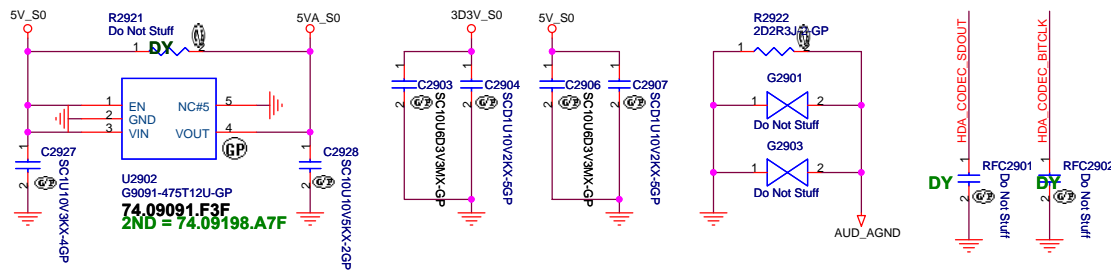


For PWM FAN



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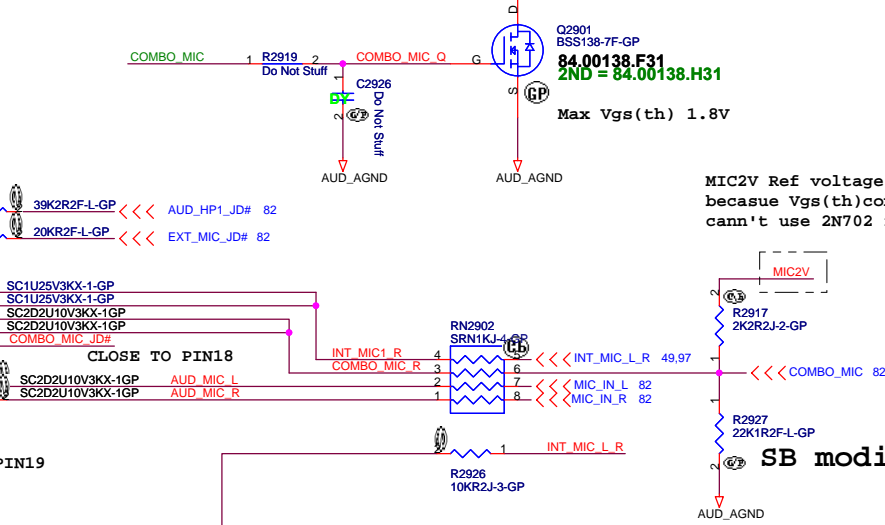
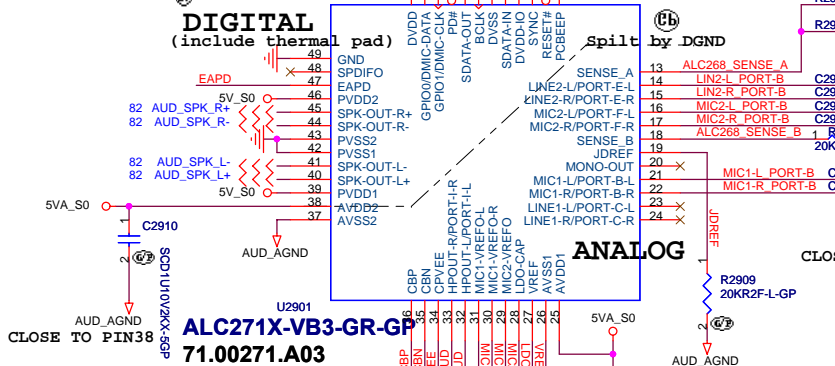
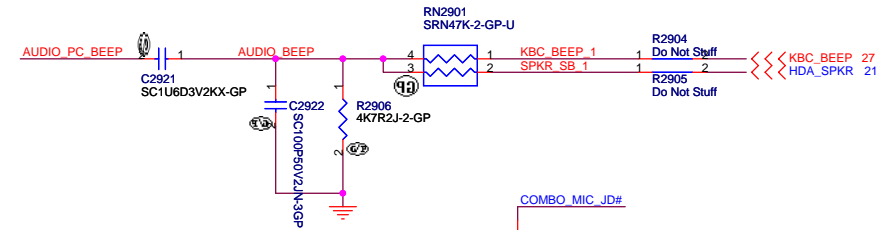
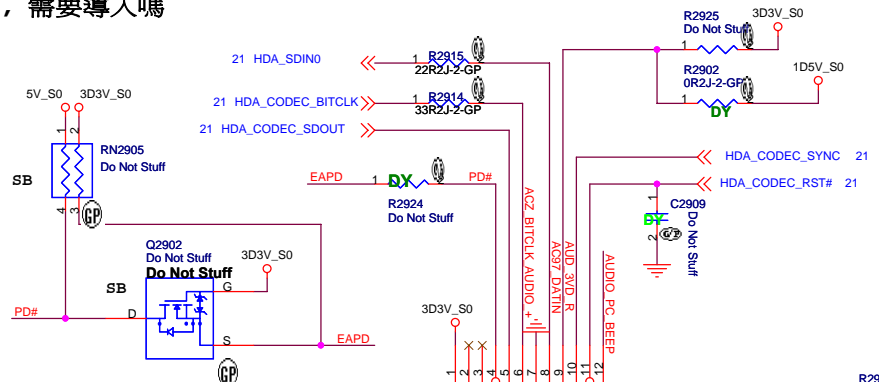
Title		Thermal P2800/Fan Controller P2793	
Size	Document Number		
Custom	JE40-HR	Rev -1	
Date:	Thursday, December 02, 2010	Sheet 28	of 102



CLOSE TO PIN39 and 46

-1 PVDD timing 需要比 AVDD晚, 使用PW 74.00545.079 去開  
vensor suggest , 需要導入嗎

CLOSE TO PIN1 and 9



MIC2V Ref voltage is 2.5V  
because Vgs(th) concern  
can't use 2N702 for desing

SB modify

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio Codec		
Size A3	Document Number	Rev
	JE40-HR	-1
Date: Thursday, December 02, 2010	Sheet 29	of 102

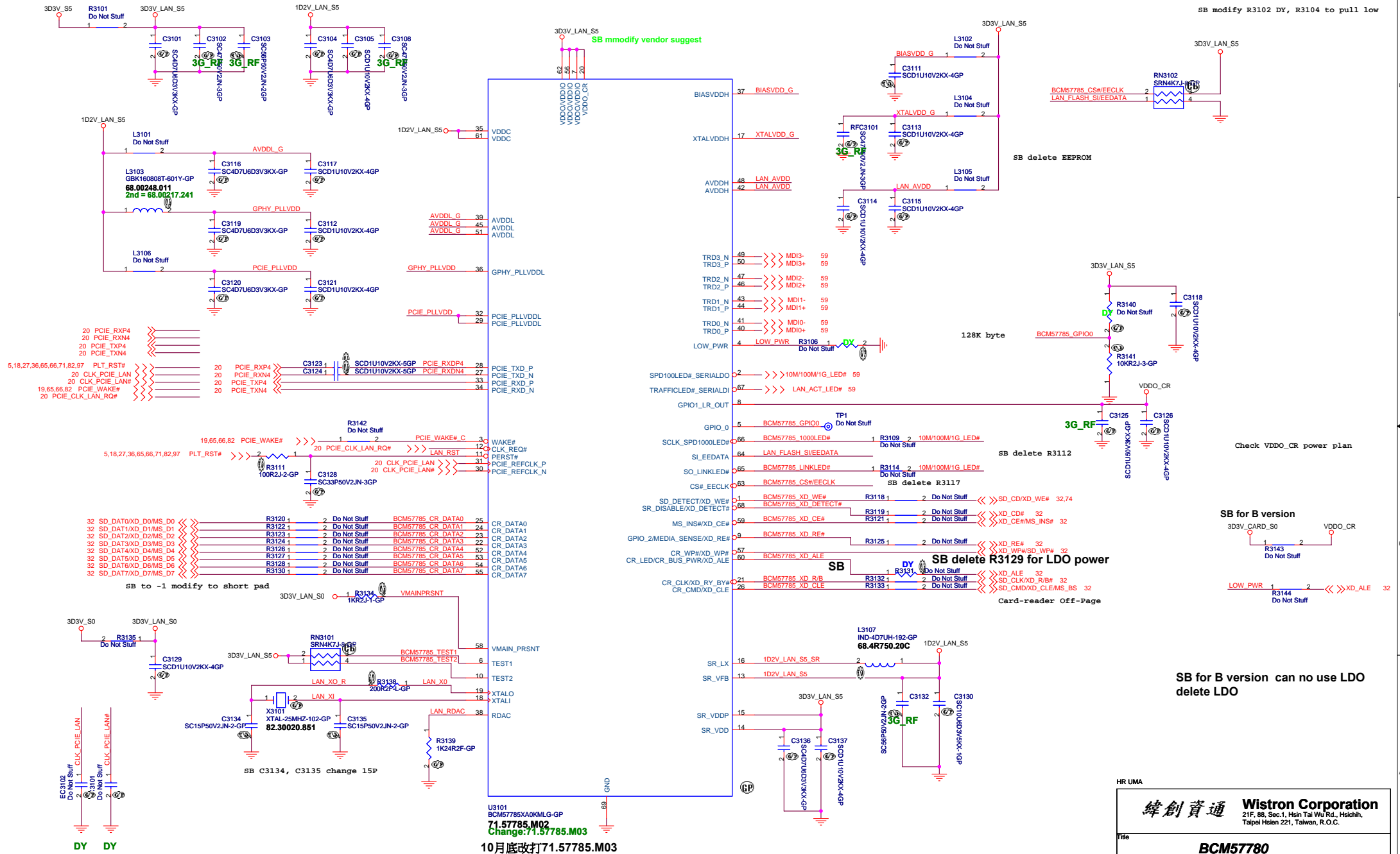
AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Audio AMP</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 30 of 102

# SB modify L3101,2,4,5,6 to 0 ohm



10月底改打71.57785.M03





(Blanking)

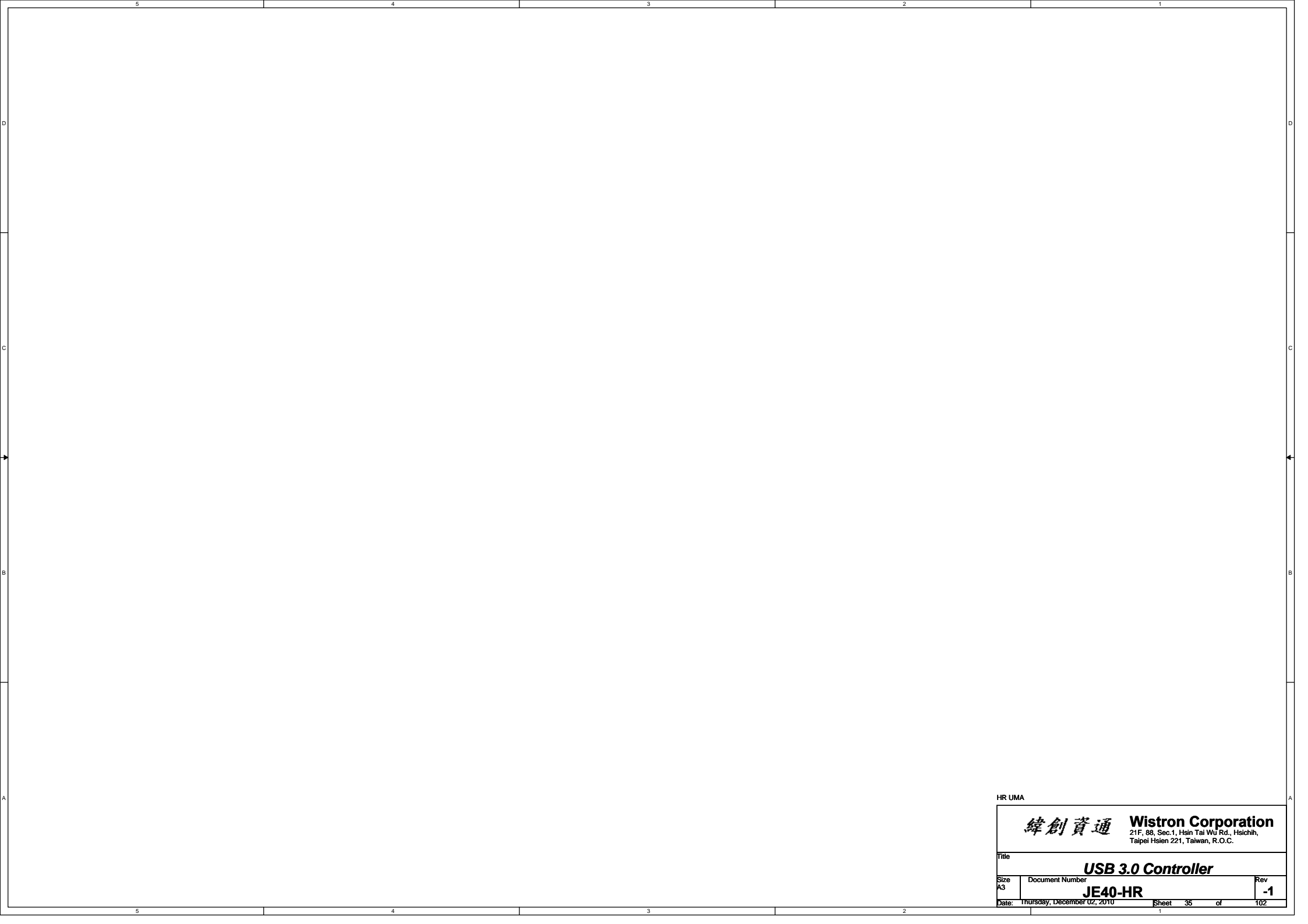
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 33 of 102

( Blanking )

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 34 of 102



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>USB 3.0 Controller</b>			
Size	Document Number		Rev
A3	<b>JE40-HR</b>		<b>-1</b>
Date:	Thursday, December 02, 2010		Sheet 35 of 102

[illegible]

**ANNIE Run Power**

**-1 co-layout SLG55221**

**-1 modify R3621,D3602 to DY**

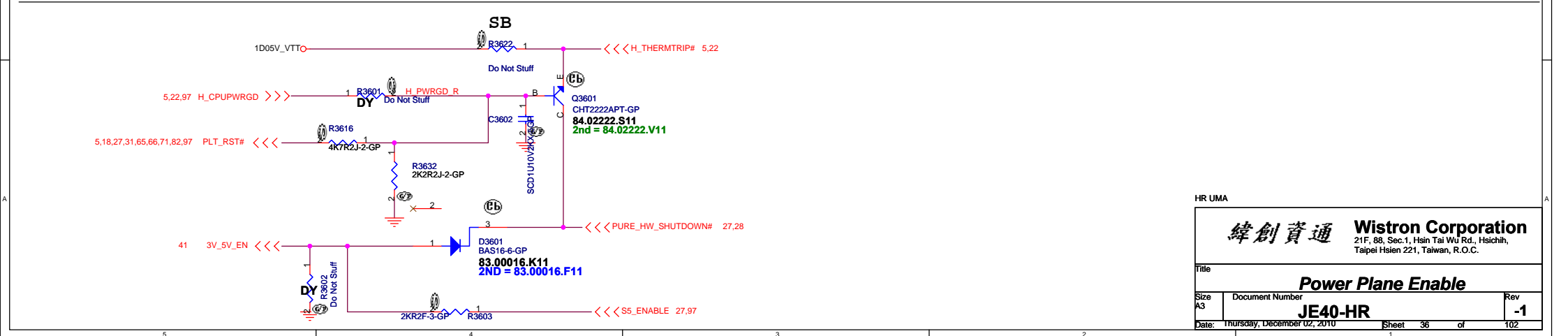
**SB modify part number**

**1D5V\_S0**

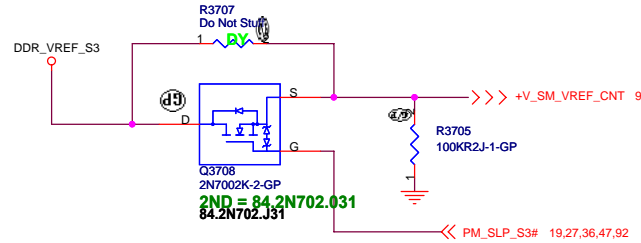
**MAX Current 3000 mA**

**Design Current 2100 mA**

**Total= 11.39A**

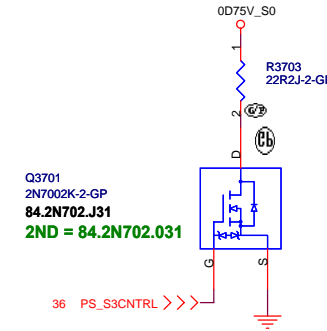


Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation

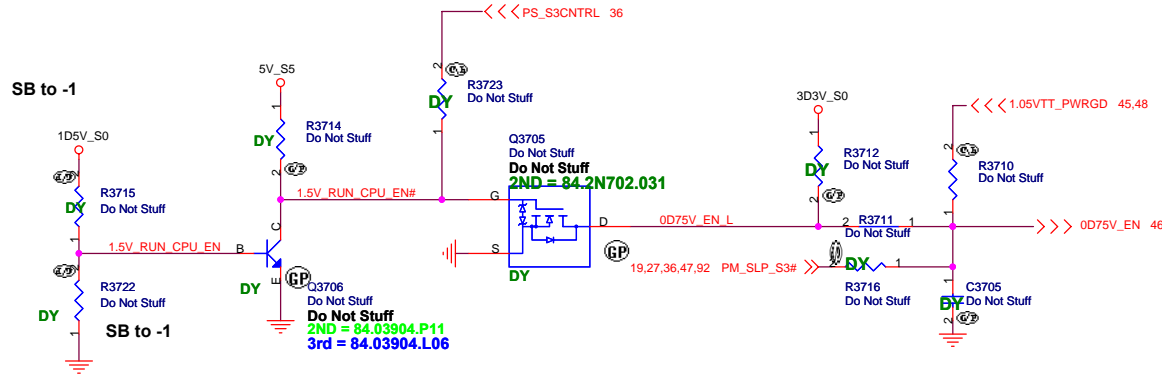


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

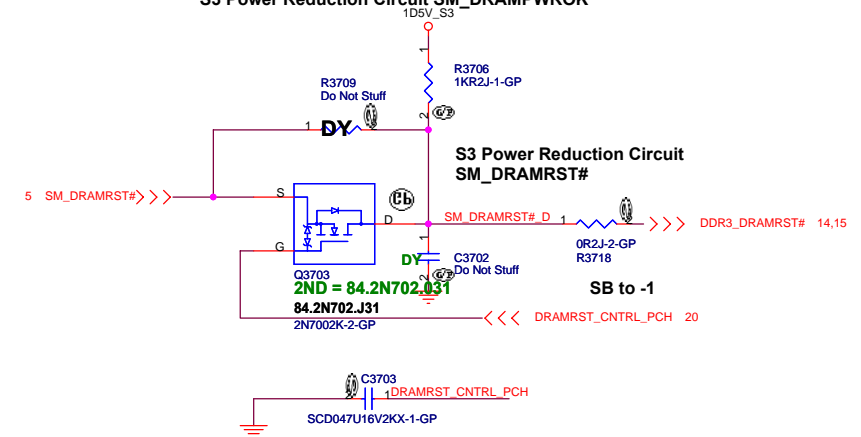
Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK



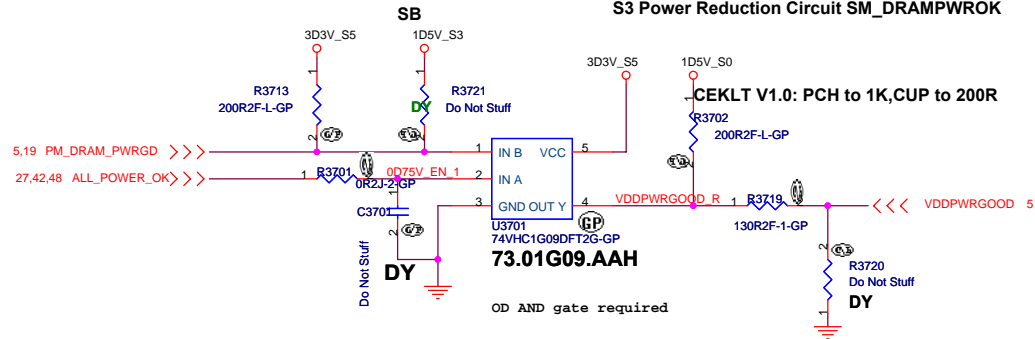
SB to -1 reserve R3723



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



For U3701 not OD AND gate  
R3719 to 64.15015.6DL  
R3720 to 64.75005.6DL  
R3702 to DY

SM\_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55± 200mV and the edge must be monotonic

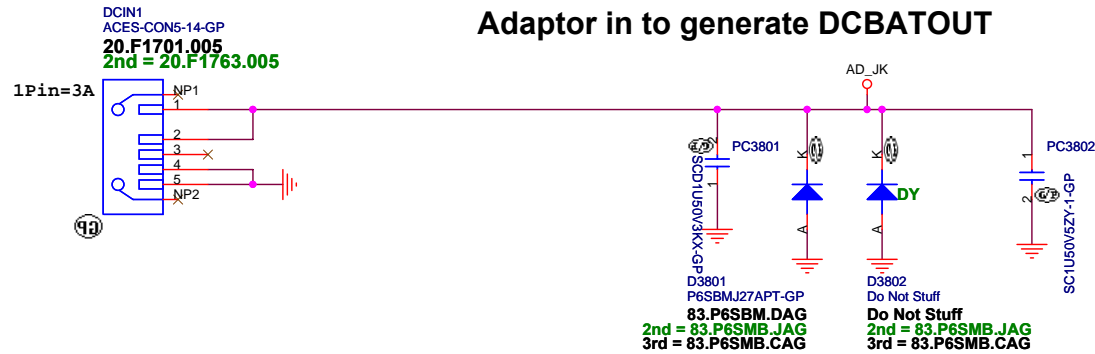
HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

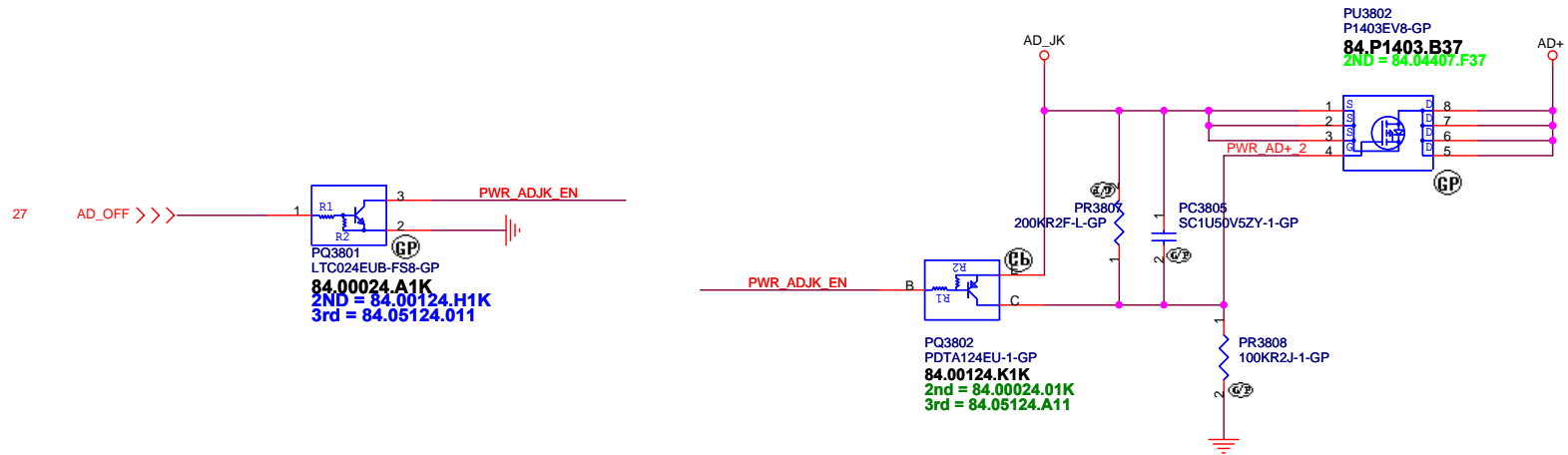
Title <b>ADAPTER</b>		
Size A3	Document Number <b>JE40-HR</b>	Rev <b>-1</b>
Date: Thursday, December 02, 2010	Sheet 37	of 102

# ANNIE solution

## Adaptor in to generate DCBATOUT



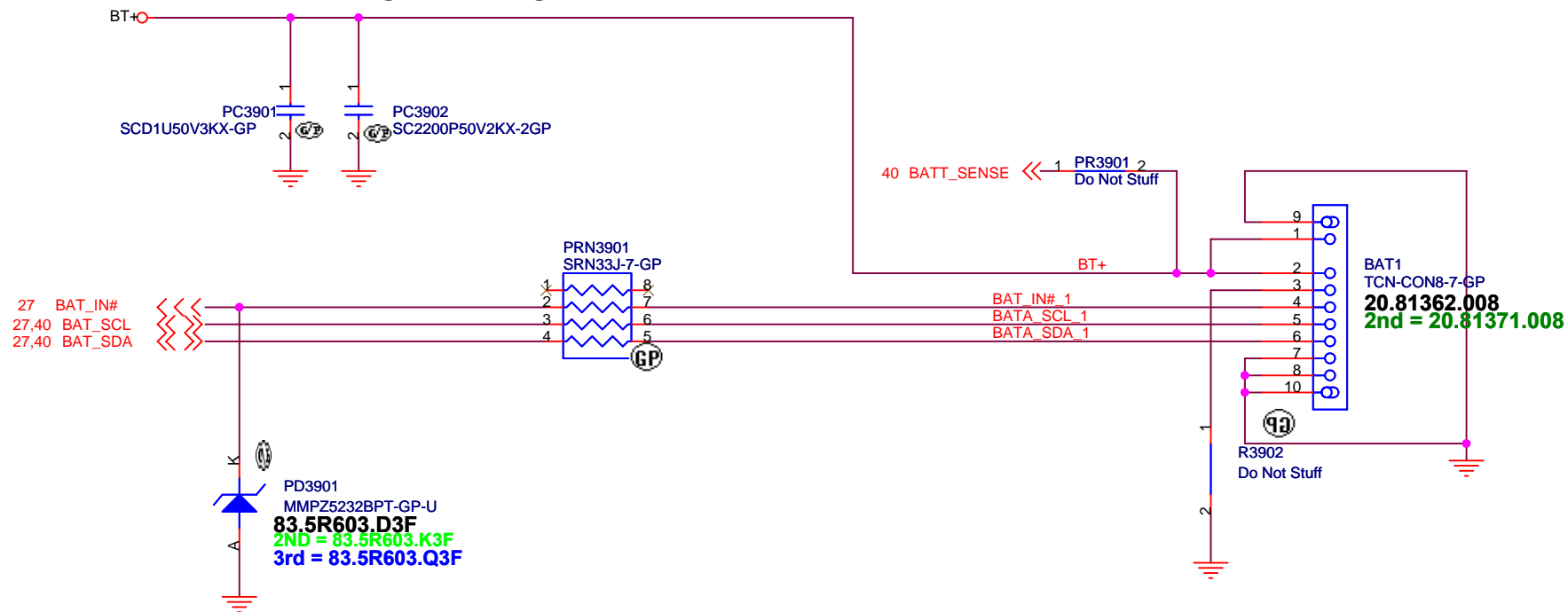
JE40 change DCIN1 part number



HR UMA

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Title			
<b>DCIN JACK</b>			
Size	Document Number		Rev
Custom	<b>JE40-HR</b>		<b>-1</b>
Date:	Thursday, December 02, 2010		Sheet 38 of 102

# BATTERY CONNECTOR



EC Protect

HR UMA

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Title

**BATT CONN**

Size  
A4

Document Number

**JE40-HR**

Rev  
**-1**

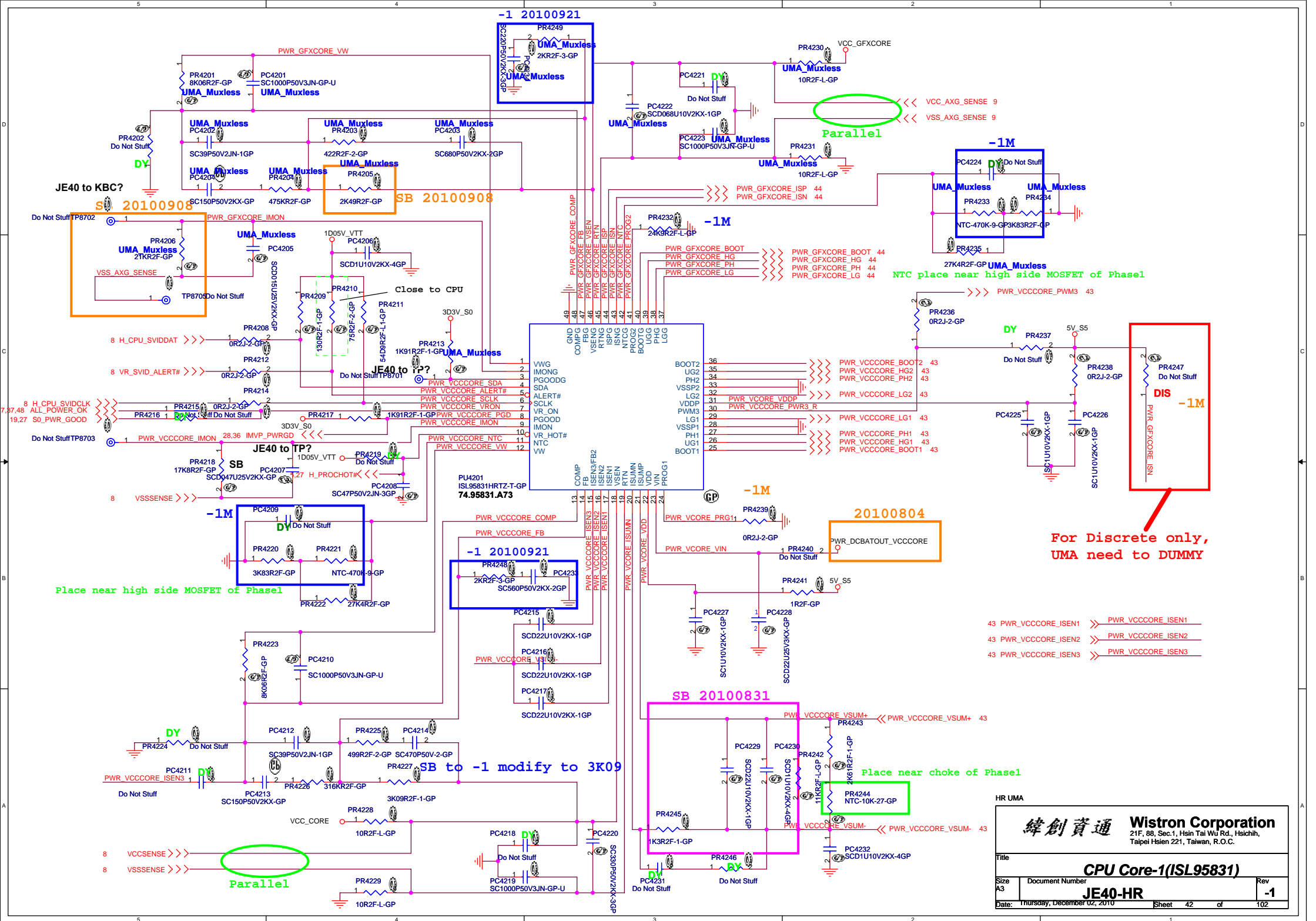
Date: Thursday, December 02, 2010

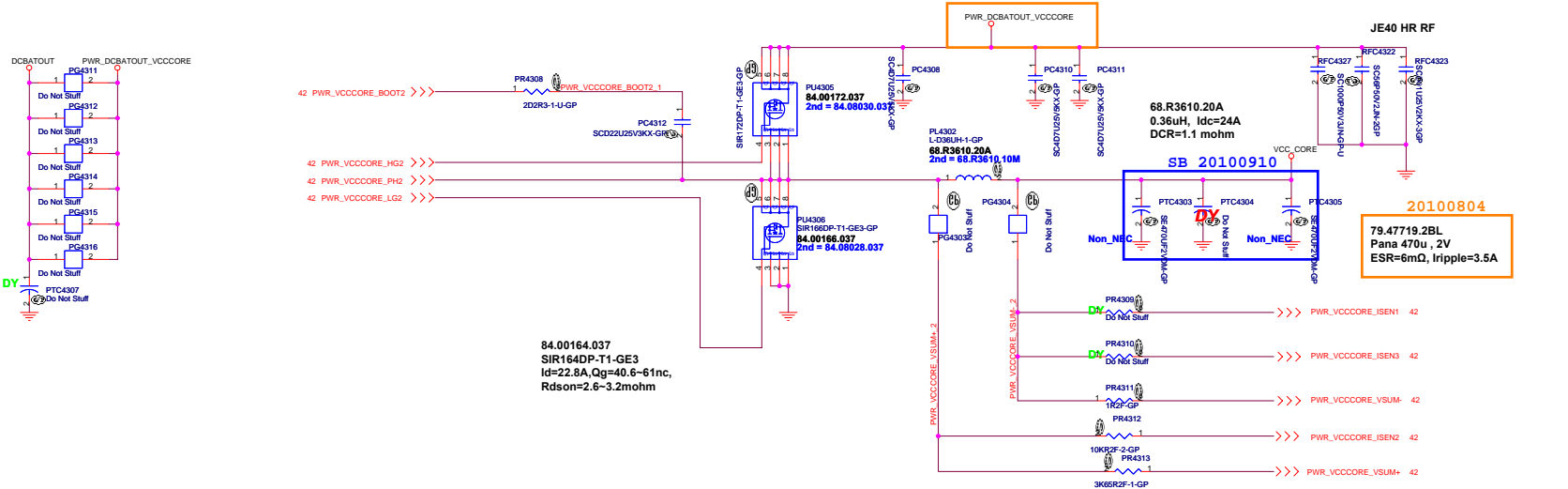
Sheet 39 of 102





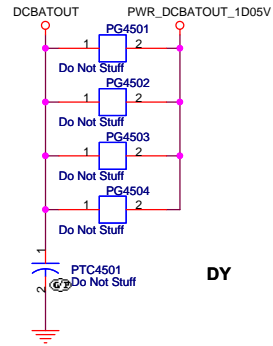




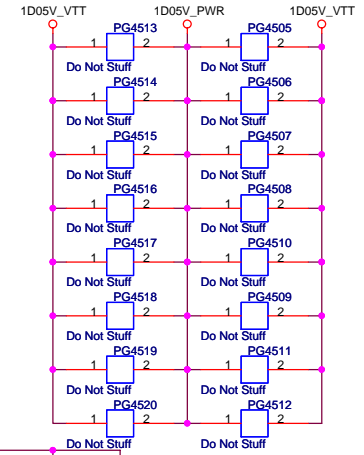
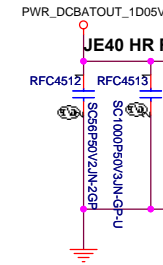




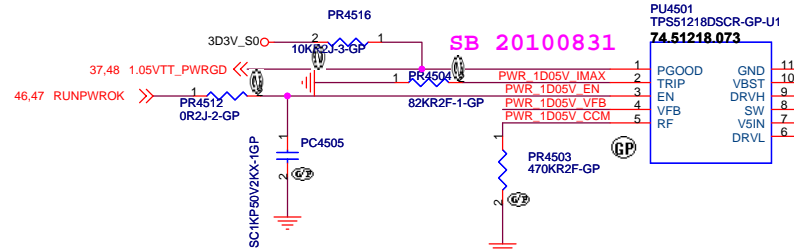
# TPS51218D for 1D05V



DY



2nd source 還未導入 74.08237.073



Freq=360KHz

20100728  
Id=12.9A  
Qg=9.8~15nC  
Rdson=10.3~12.4mohm

PU4502  
84.15N03.037  
2nd = 84.08065.037

20100728  
Iomax=14A  
OCP>21A

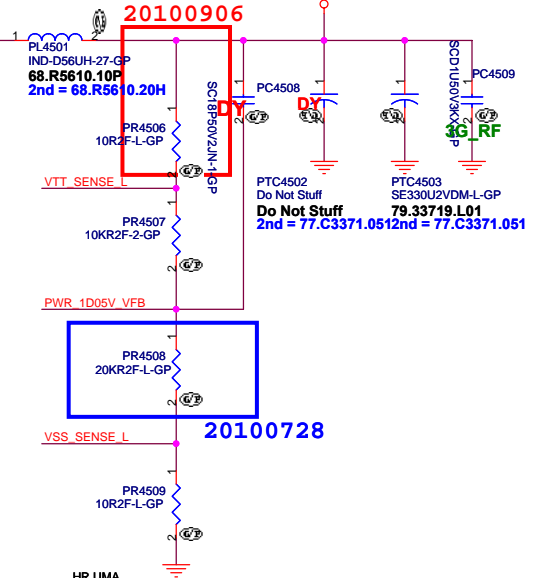
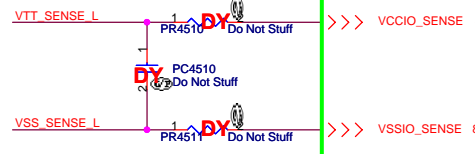
Mag. 0.56uH 10\*10\*4  
DCR=1.6~1.8mohm  
Idc=25A, Isat=40A

20100728

Id=19.4A  
Qg=16.8~25.5nC  
Rdson=4.9~6.1mohm

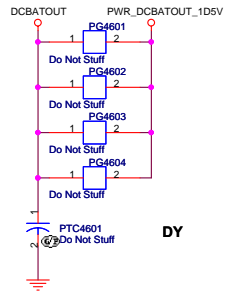
20100728

Vout=0.704\*(1+R1/R2)



HR UMA

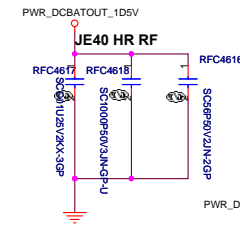
```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



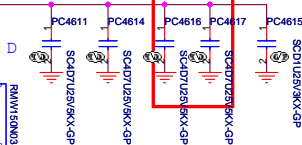
**DY**

20100805

## RT8207L for 1D5V

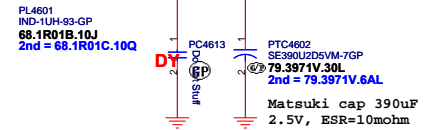


20100906

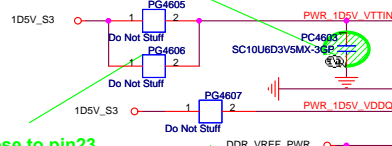


Mag. 1.0uH 10\*10\*4 Iomax=12A  
DCR=2.9~3.3mohm OCP>20A  
Idc=18A, Isat=36A

Iomax=12A  
OCP>20A


$$V_{out} = 0.75 * (1 + R1/R2)$$

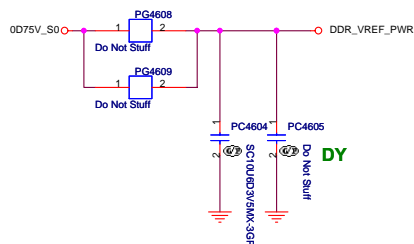

20100728



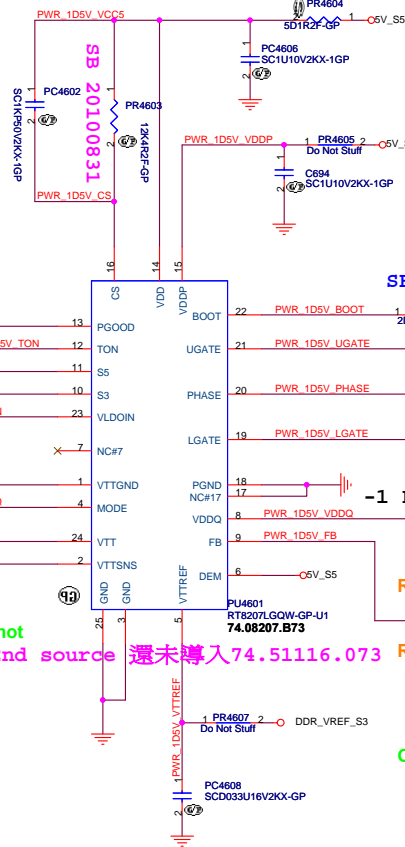
20100728  
Iomax=1A  
OCP>1.5A

Close to output cap pin1, not inside of the output cap 2nd source 還未導入 74.51116.073

**+0.75VS**  
**Iomax: 1.2A**



DY



20100728

Id=12.9A  
Qg=9.8~15nC  
Rdson=10.3~12.4mohm

-1 PR4608 需要將來都改32k+1 為 84.180

### Close to PIN9

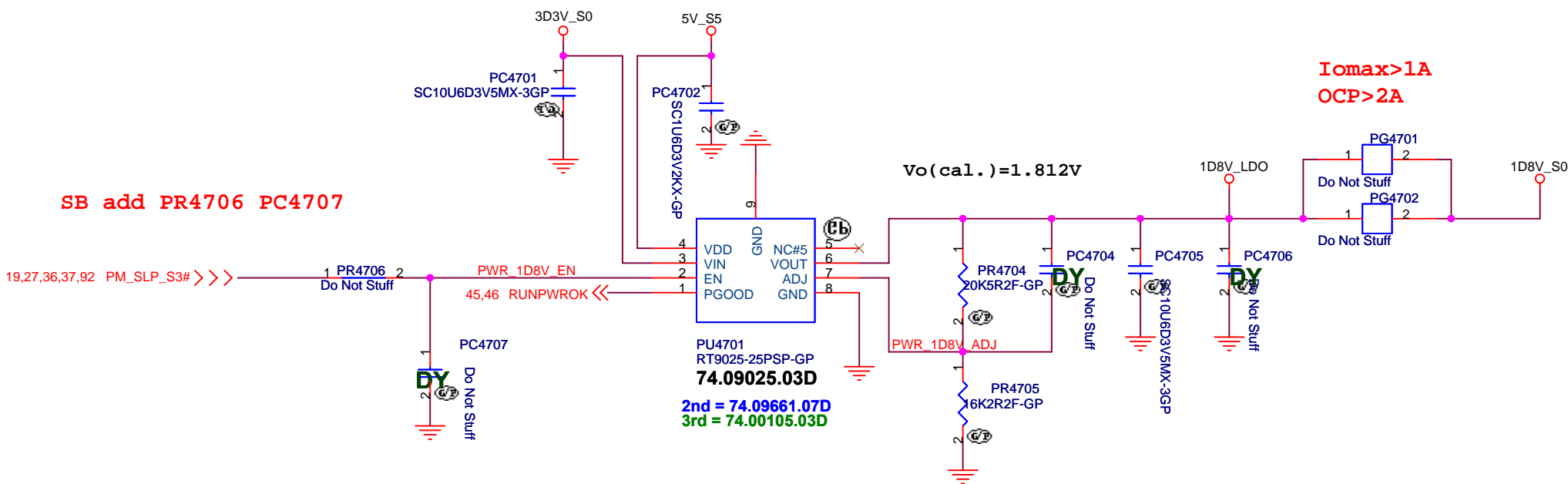
20100728

Id=19.4A  
Qg=16.8~25.5nC  
Rdson=4.9~6.1mohm

SB R4608 chekc 修改31K6R  
Vout 需再1.55V 以上

SSID = PWR.Plane.Regulator\_1p8v

RT9025 for 1D8V\_S0

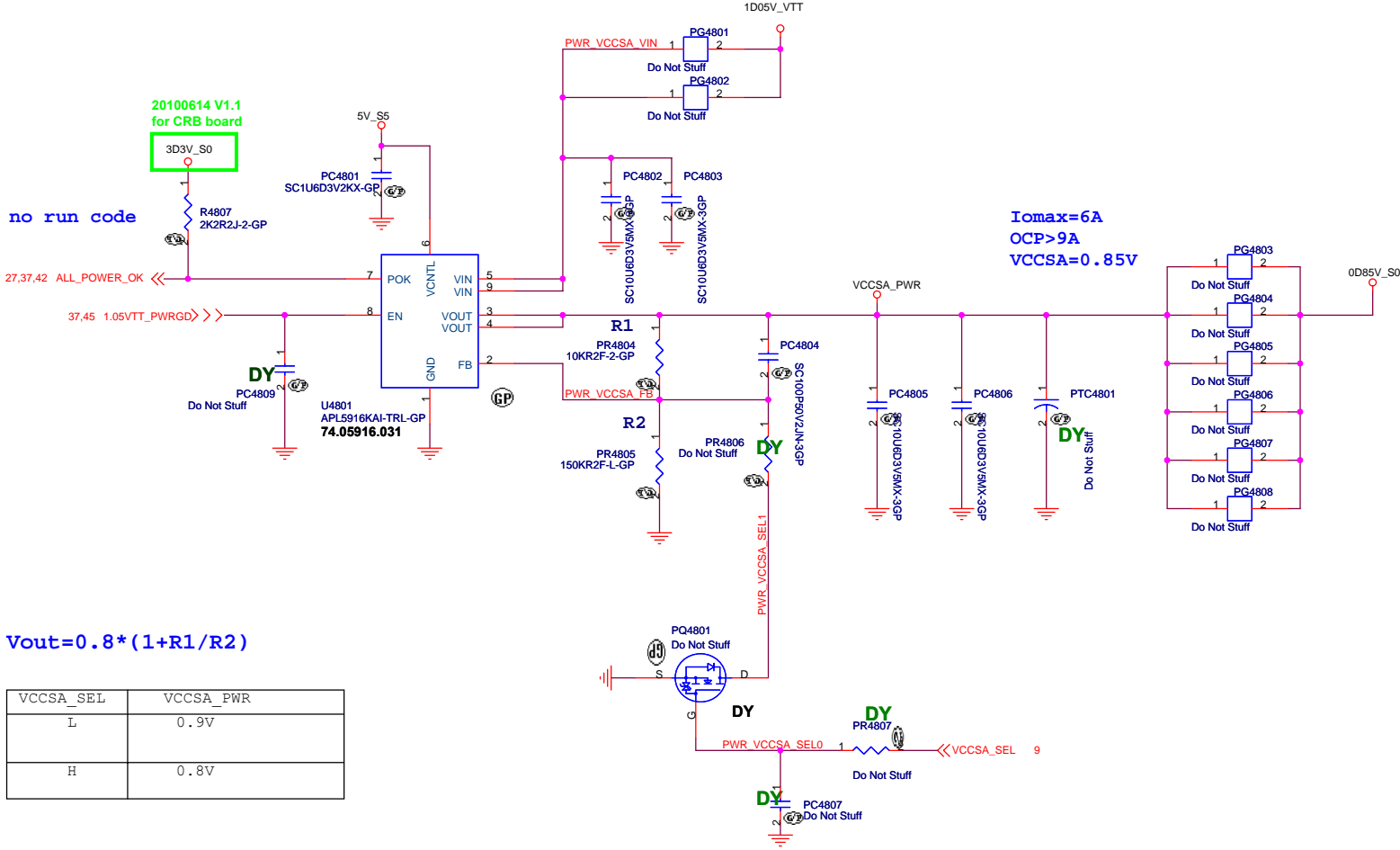


HR UMA

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Title			
<div>LDO 1D8V(RT9025)</div>			
Size A4	Document Number <div>JE40-HR</div>		Rev <div>-1</div>
Date:	Thursday, December 02, 2010	Sheet 47 of	102
2		1	

APL5916 for VCCSA

SB modify 2K2 for no run code



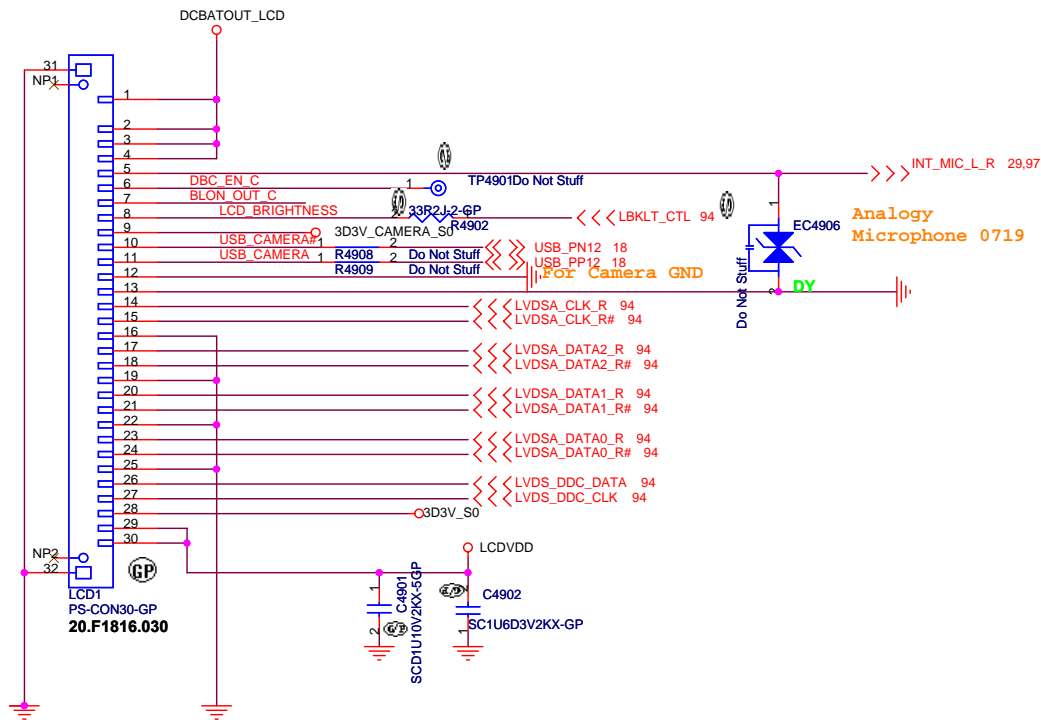
$V_{out}=0.8*(1+R1/R2)$

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V



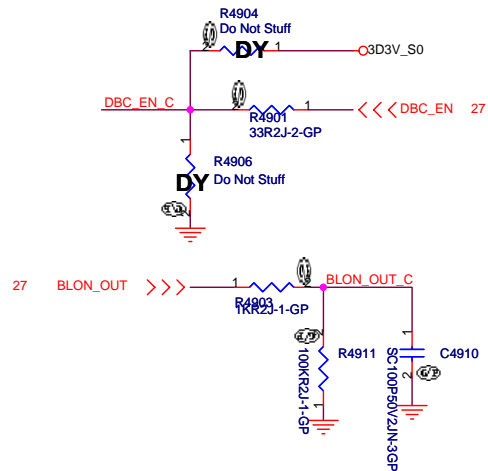
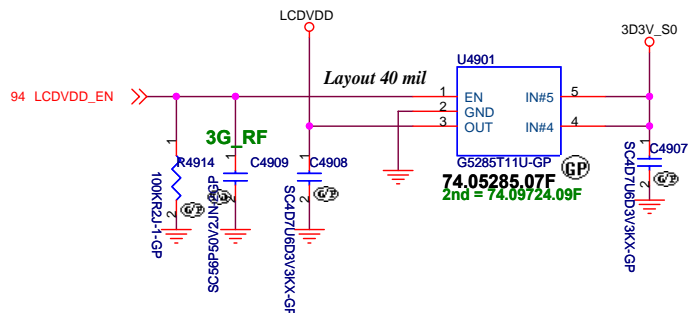
**SSID = VIDEO**

## LVDS CONNECTOR

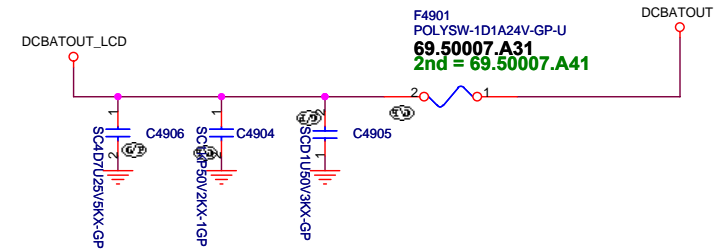


**SSID = VIDEO**

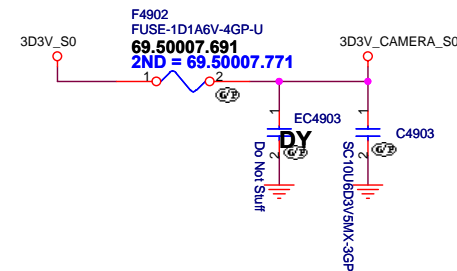
LCD POWER for ANNIE



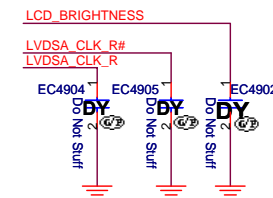
## INVERTER POWER



## Camera Power



For EMI request  
Close to LVDS connector



HR UMA

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
Title	Author	Date	Location	Notes
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Title	Author	Date	Location	

### ***LCD Connector***

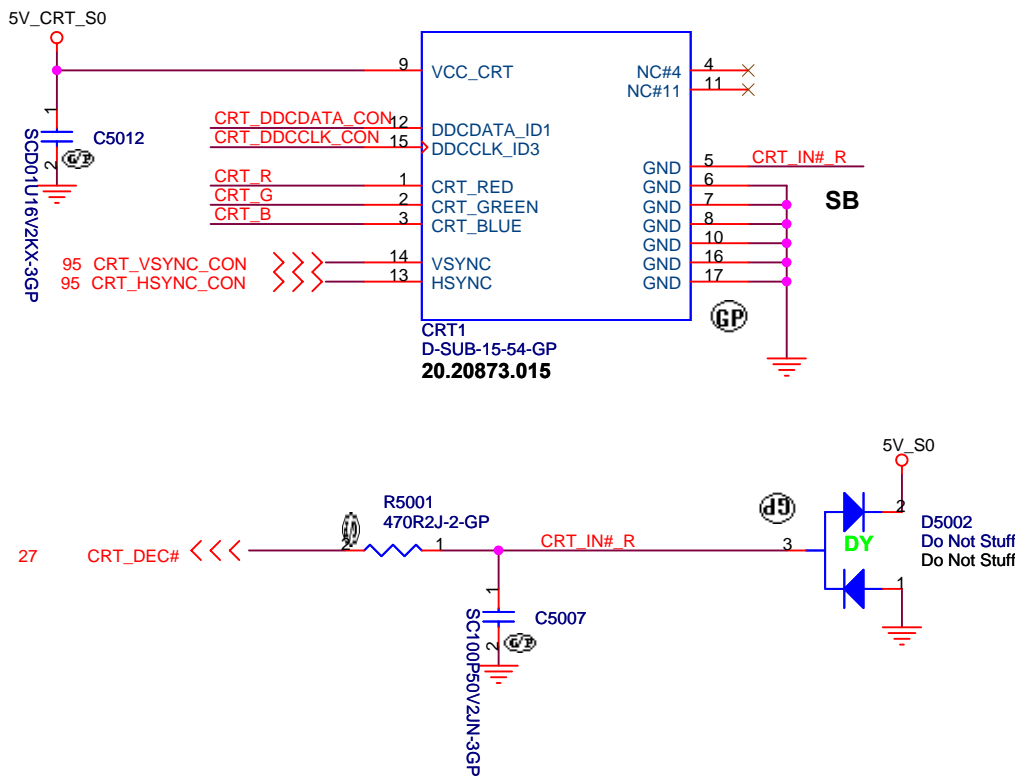
Size	Document Number
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**JE40-HR**

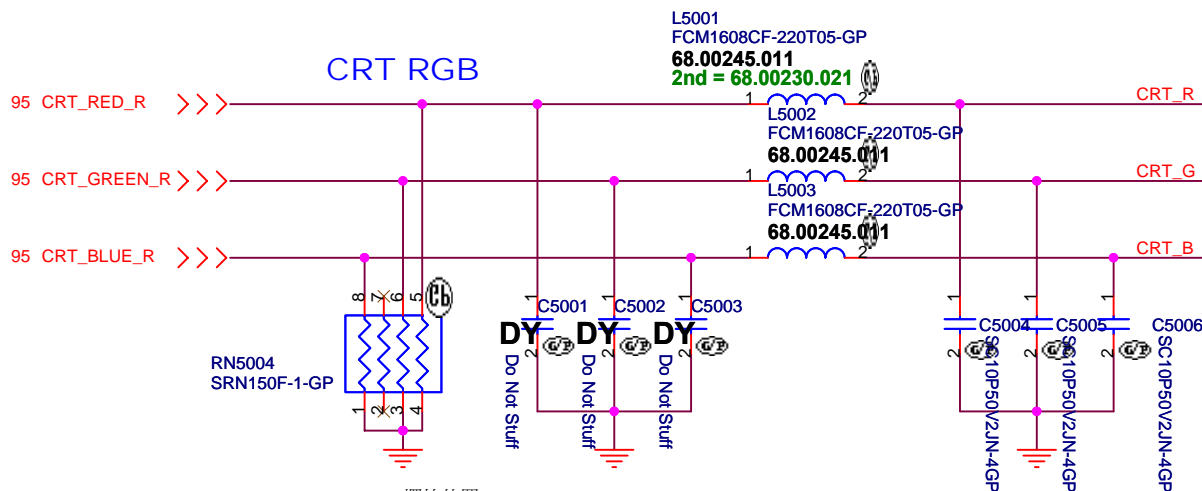
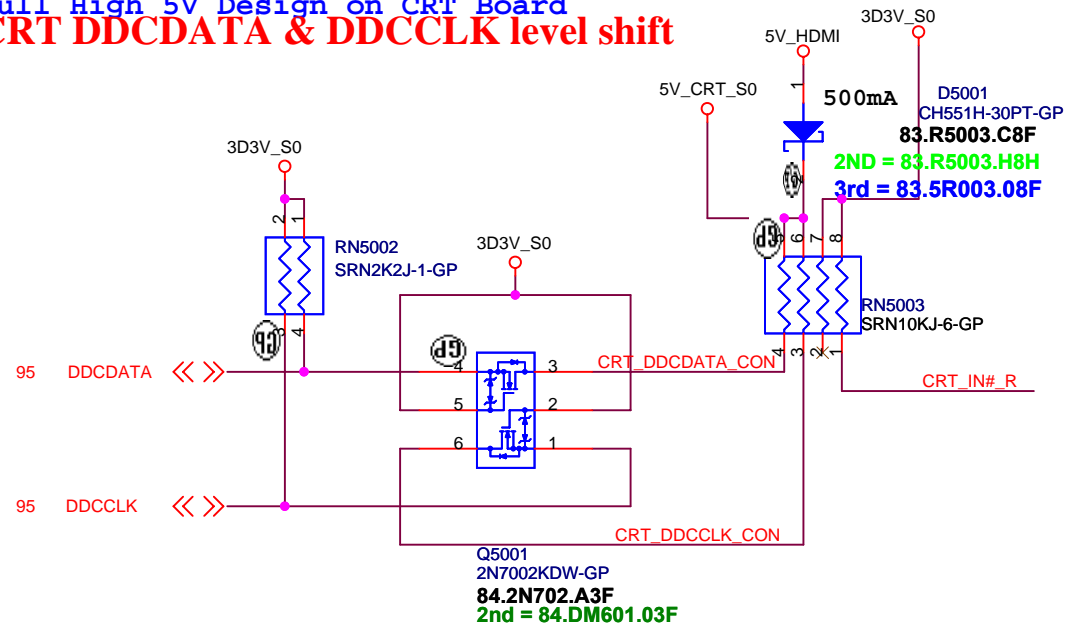
Date: Thursday, December 02, 2010

Sheet 49 of 102

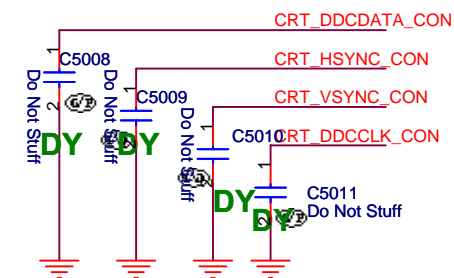
Rev  
-1



## Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift



0806 check RN5004 擺放位置



HR UMA

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CRT Connector**

Size  
A4

Document Number

**JE40-HR**

Rev

**-1**

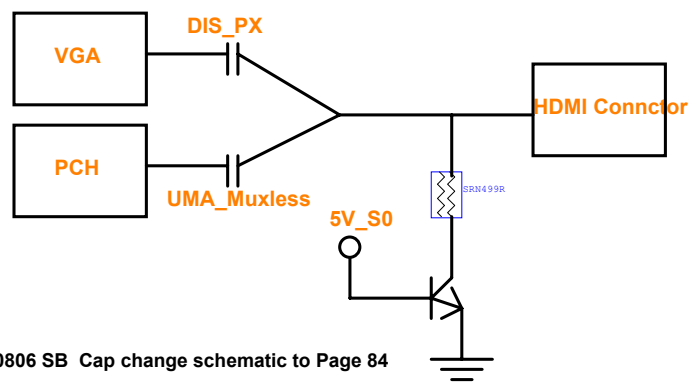
Date: Thursday, December 02, 2010

Sheet 50 of 102

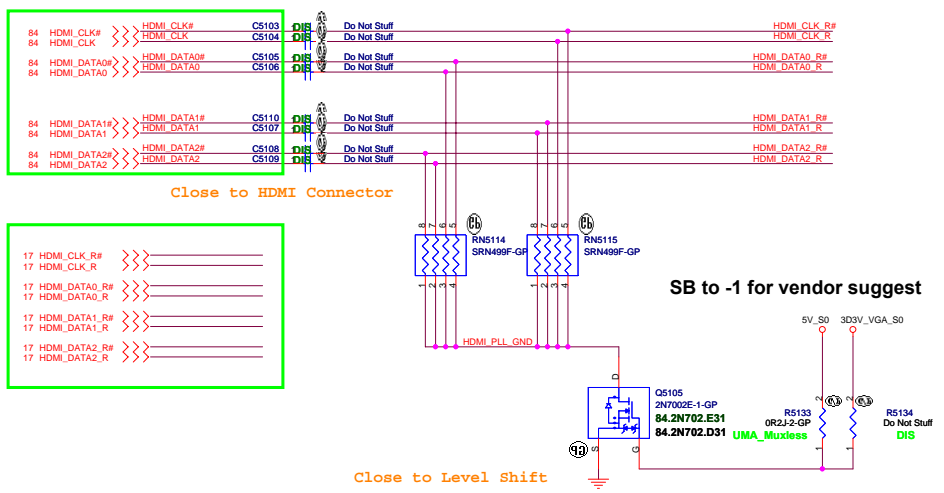
# SSID = VIDEO HDMI Level Shifter & CONNECTOR

UMA\_Muxless : default setting used PS8101. if don't used PS8101  
please change C5103-C5110 to 0 ohm resistor

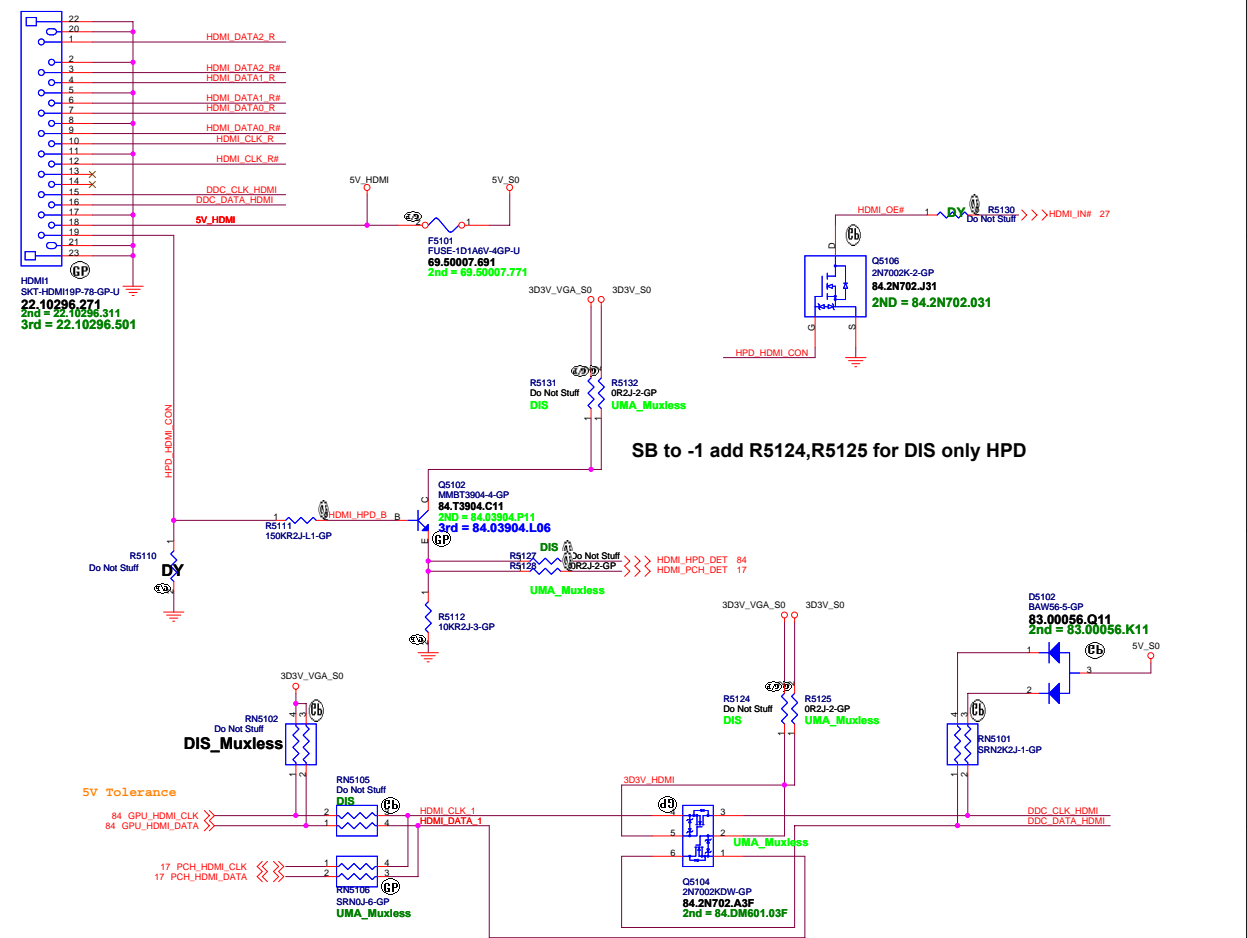
## HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



## HDMI CONN



LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
eDP			
Size	Document Number		Rev
A3	JE40-HR		-1
Date:	Thursday, December 02, 2010		Sheet 52 of 102

( Blanking )

HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
S-VIDEO		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 53 of 102

(Blanking)

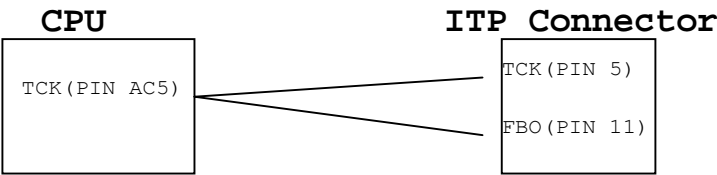
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 54 of 102


SSID = User.Interface

# ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

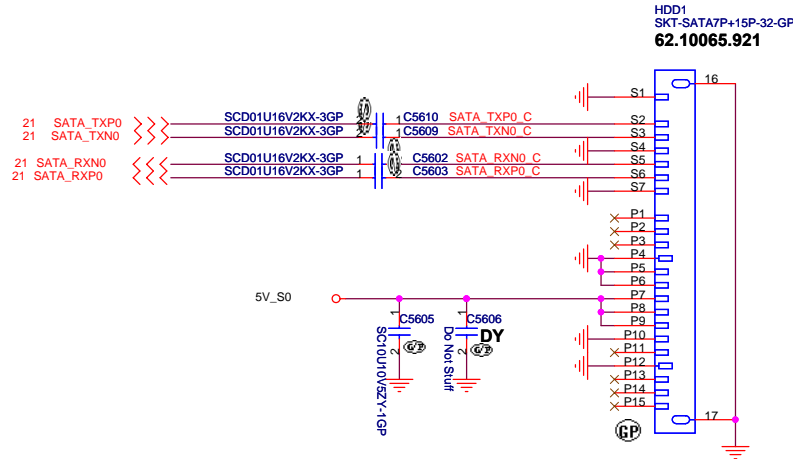


HR UMA

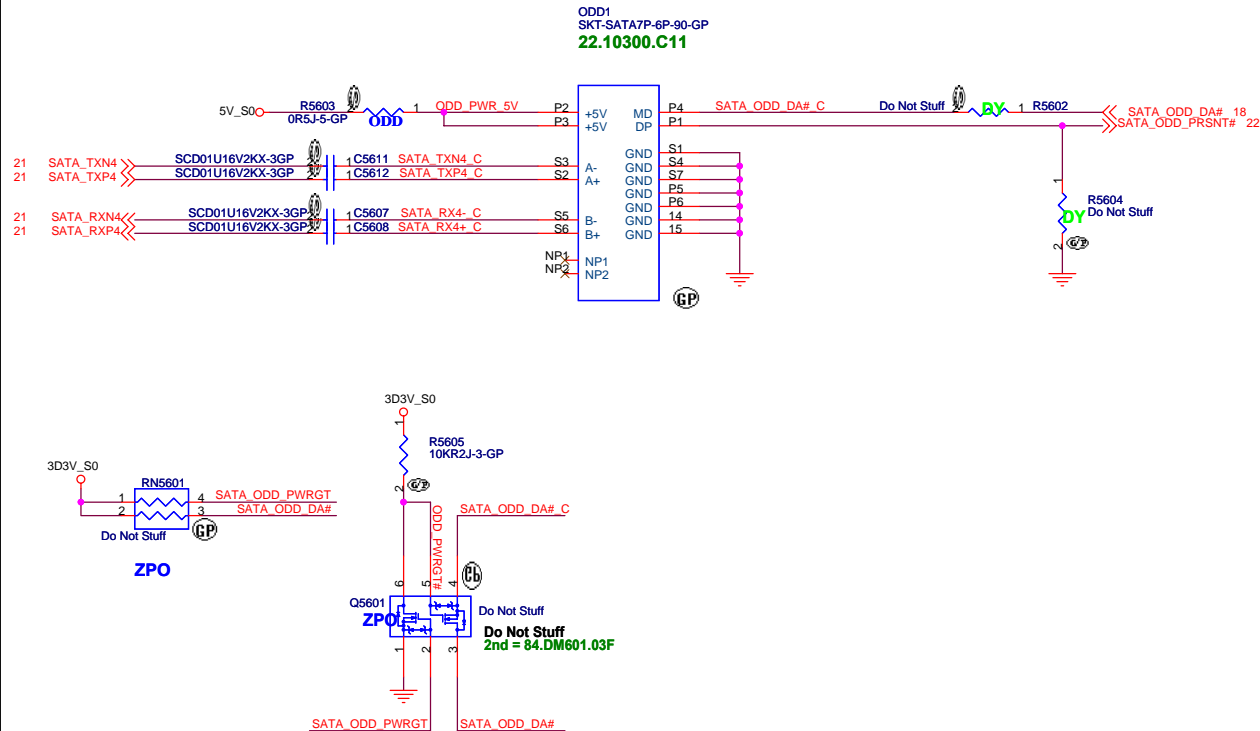
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>ITP</b>			
Size A4	Document Number <b>JE40-HR</b>		Rev <b>-1</b>
Date: Thursday, December 02, 2010		Sheet 55 of	102

SSID = SATA

# SATA HDD Connector



## ODD Connector

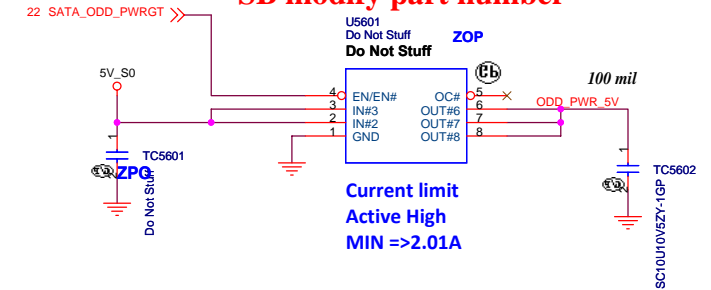


0707 Modify:  
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA



ESATA Power

USB CHARGER

HR UMA

緯創資通

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Title

Size

A3

Document Number

Date: Thursday, December 02, 2010

Sheet 57 of 102

Rev

-1

E-SATA/USB CHARGER

JE40-HR

SSID = AUDIO

Speaker Connector

LINE1 OUT  
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

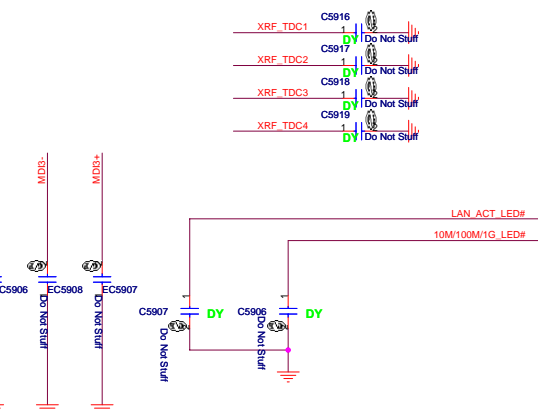
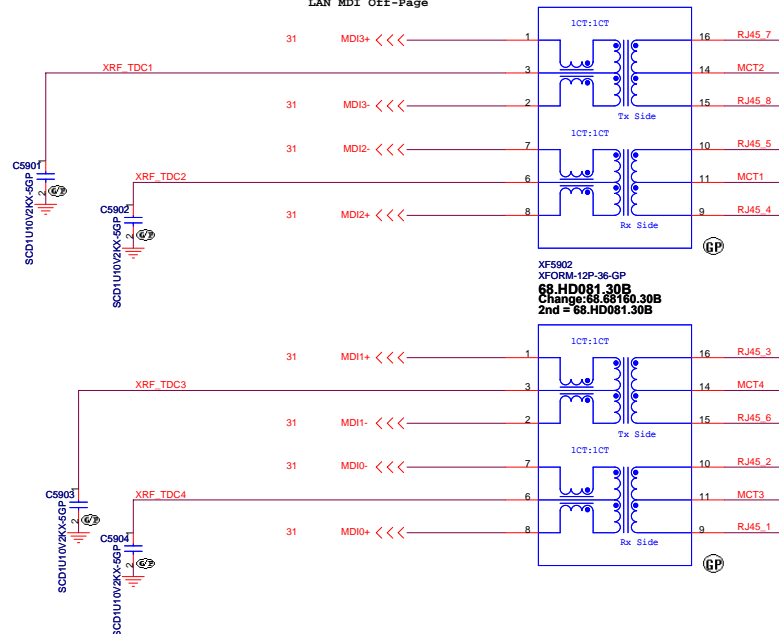
Internal  
Microphone

JE40 delete Line in function

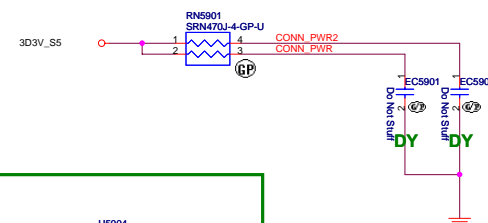
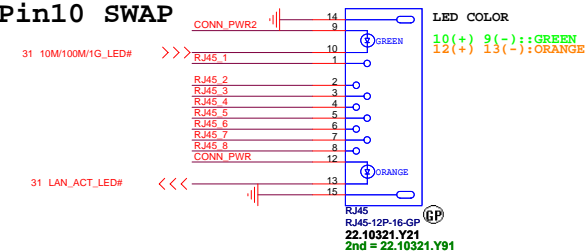
### GIGA Lan Transformer

XF5901  
XFORM-12P-36-GP  
**68.HD081.30B**  
Change:68.68160.30B  
2nd = 68.HD081.30B

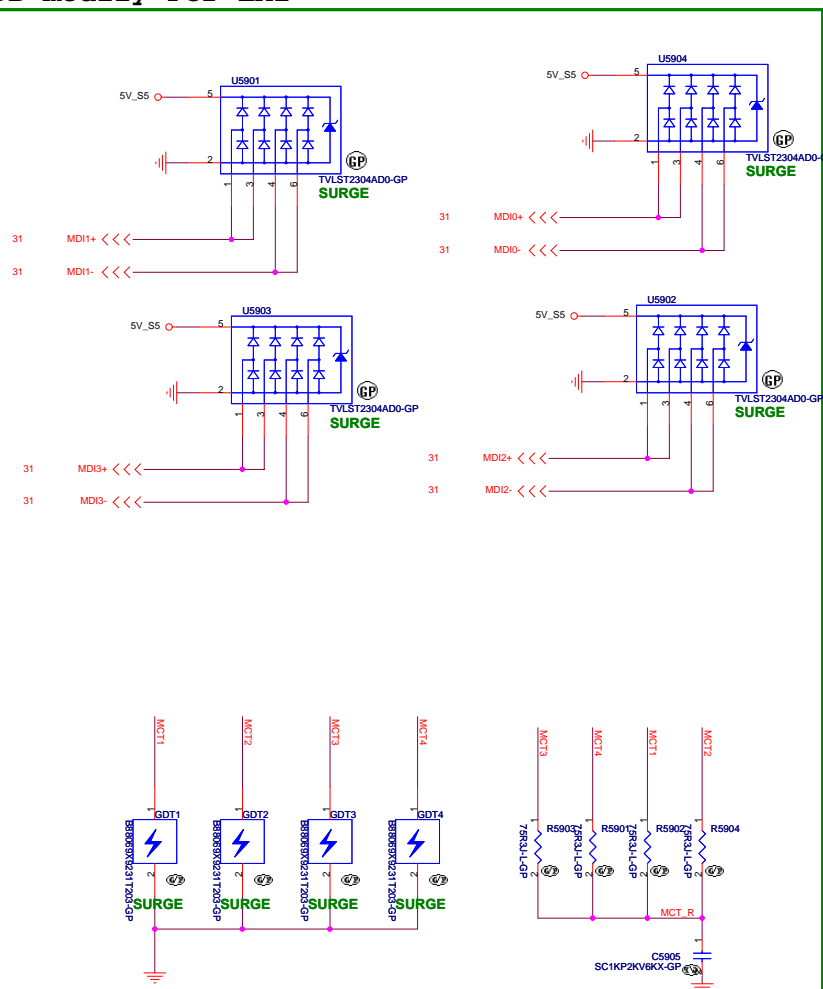
LAN MDI Off-Page



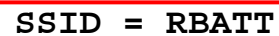
SB modiyf Pin9 Pin10 SWAP



SB modify For EMI



**SSID = Flash.ROM**



緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

### Flash/RTC

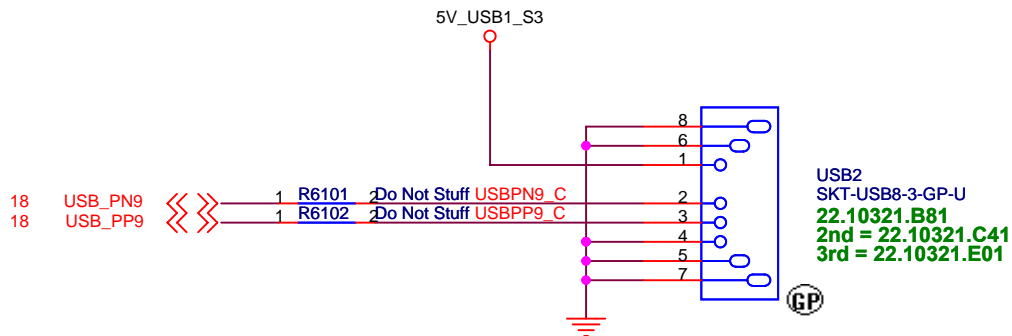
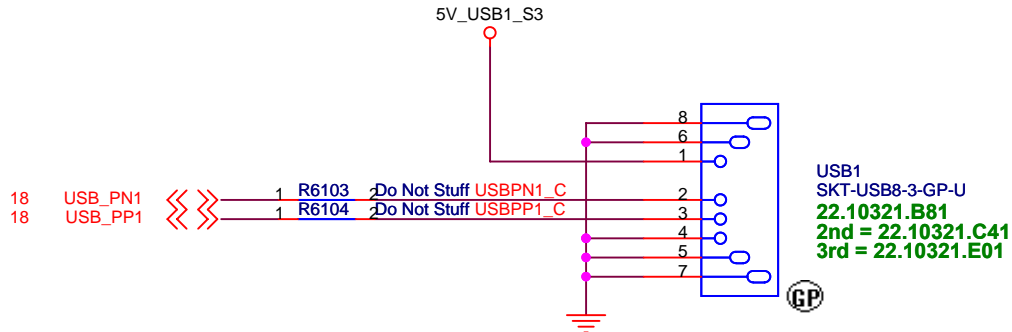
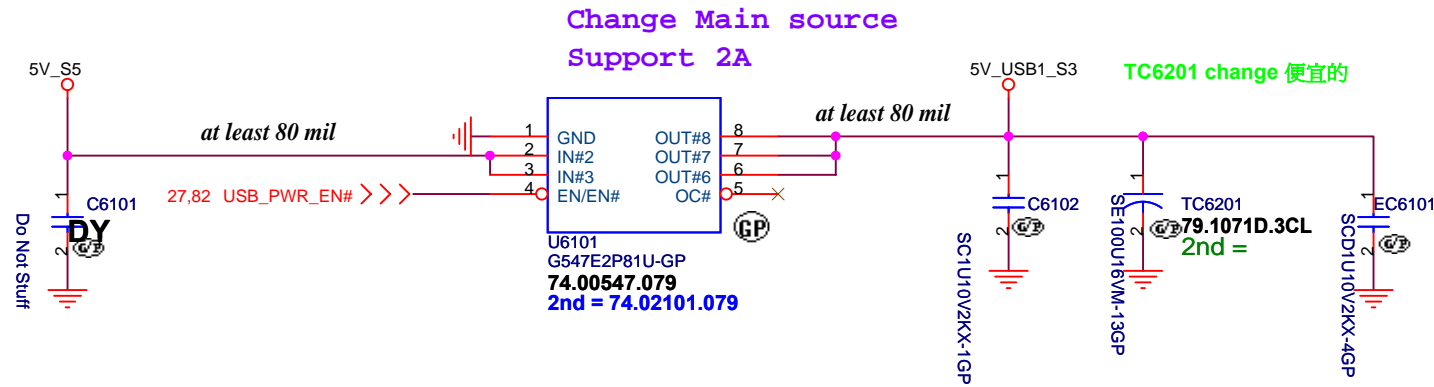
Size	Document Number	Rev
Custom	<b>JE40-HR</b>	<b>-1</b>
Date:	Thursday, December 02, 2010	Sheet 60 of 102

# JE40-HR

# JE40-HR

SSID = USB

## IO Board USB Power



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size  
A4

Document Number

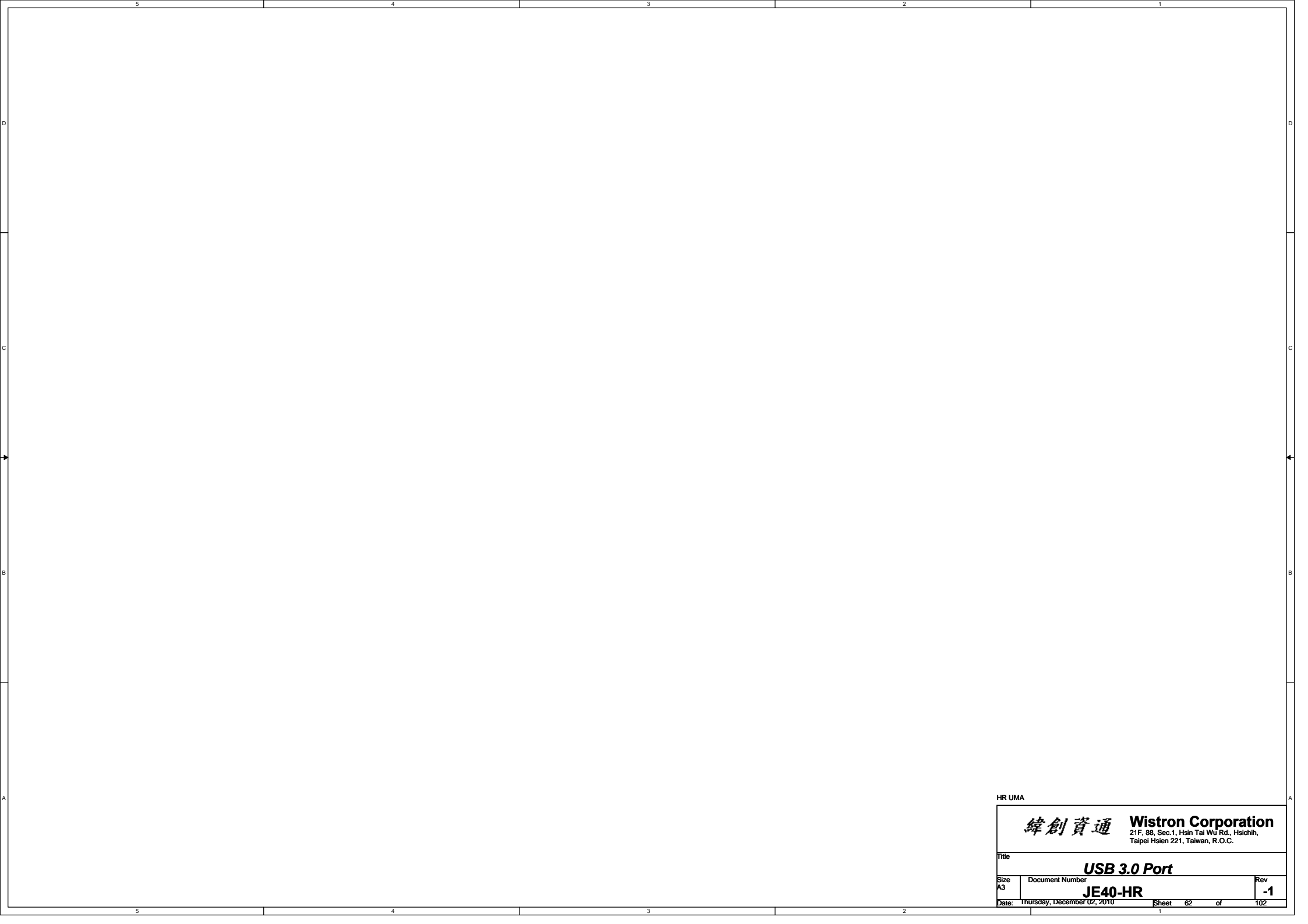
JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

Sheet 61 of 102

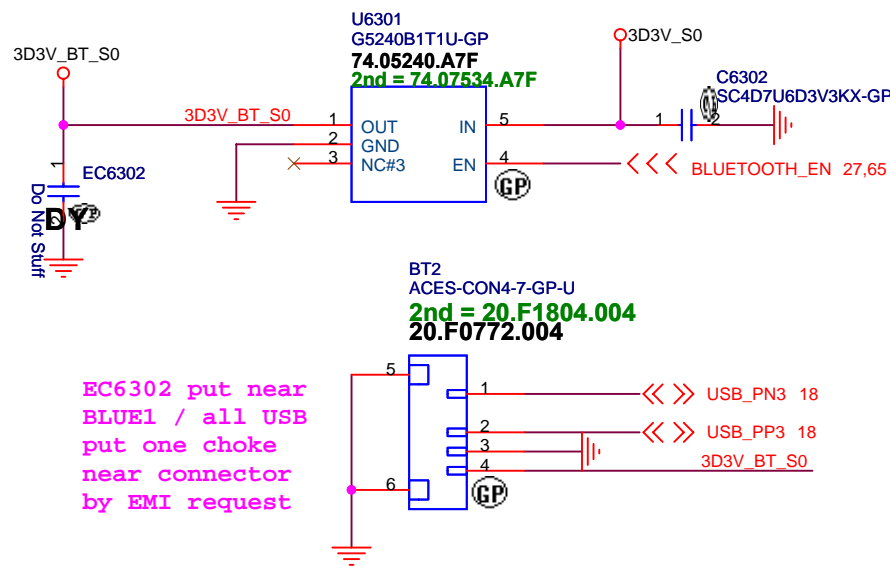


HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>USB 3.0 Port</div>	
Size <div>A3</div>	Document Number <div>JE40-HR</div>
Date: <div>Thursday, December 02, 2010</div>	Rev <div>-1</div>
Sheet 62 of 102	

SSID = User.Interface  
Bluetooth Module conn.

ANNIE Bluetooth Module

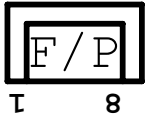


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Bluetooth			
Size	Document Number	Rev	
A4	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	63 of 102

Finger printer

JE40 delete FP function



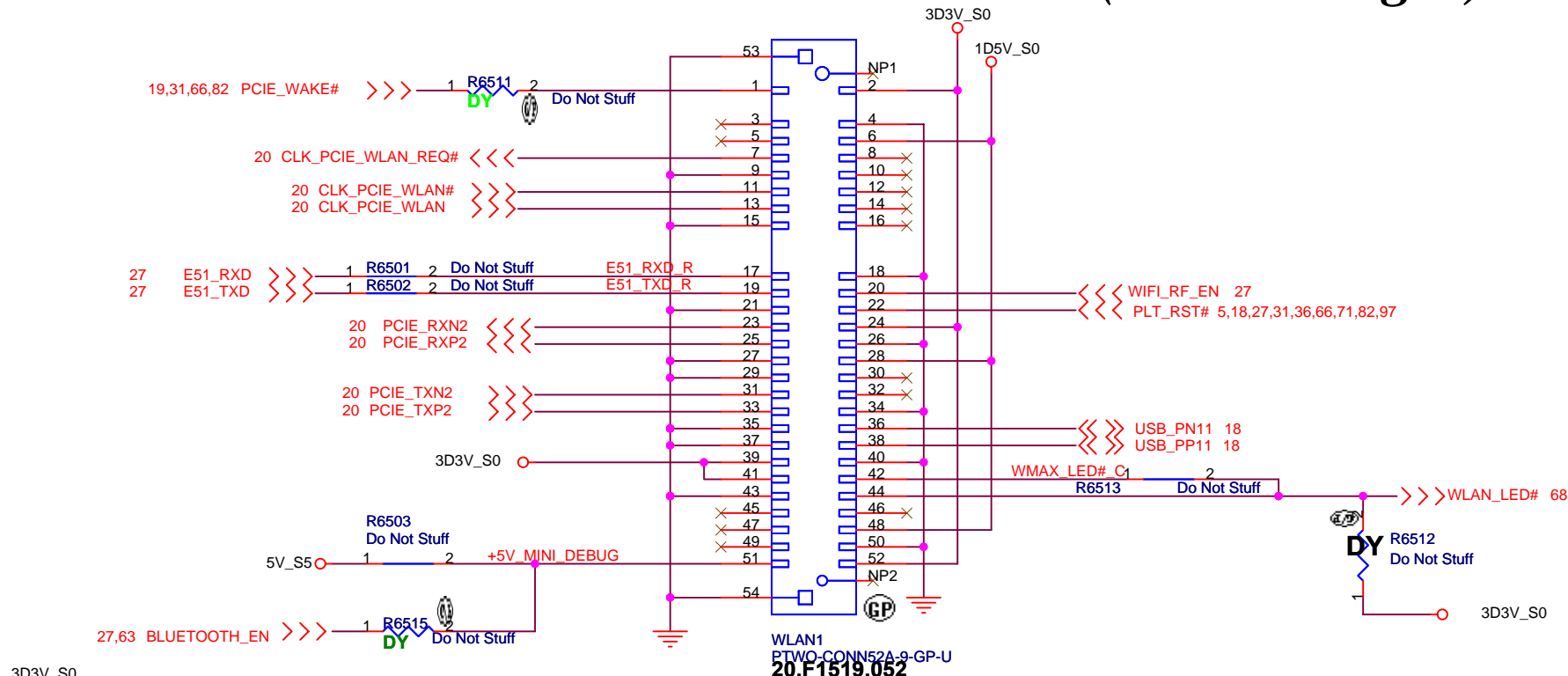
HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>RESERVED</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date <div>Thursday, December 02, 2010</div>		Sheet <div>64</div> of <div>102</div>



SSID = Wireless

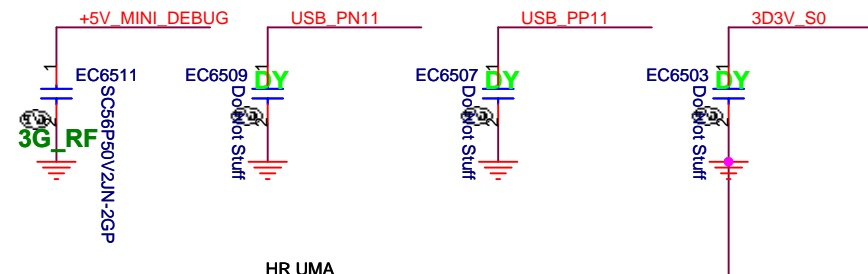
# Mini Card Connector(802.11a/b/g/n)



WLAN1  
BTW0-CONN52A-9-GP-U  
20.F1519.052  
2nd = 62.10043.A51  
3rd = 20.F1693.052  
4th = 20.F1743.052

SB modify for SIV

RF suggestion



HR UMA

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

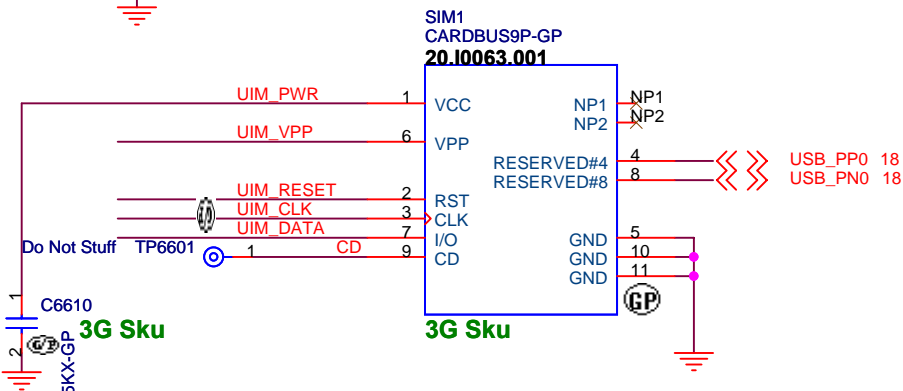
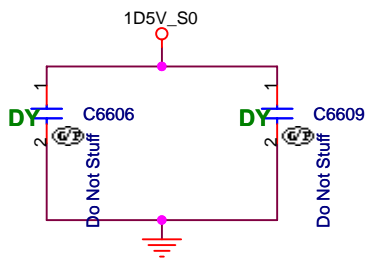
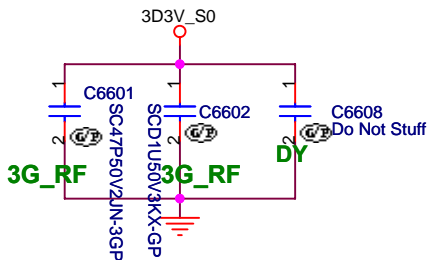
Title		
MINICARD(WLAN)/ITP CONN		
Size	Document Number	Rev
A4	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 65 of 102

**SSID = Wireless**

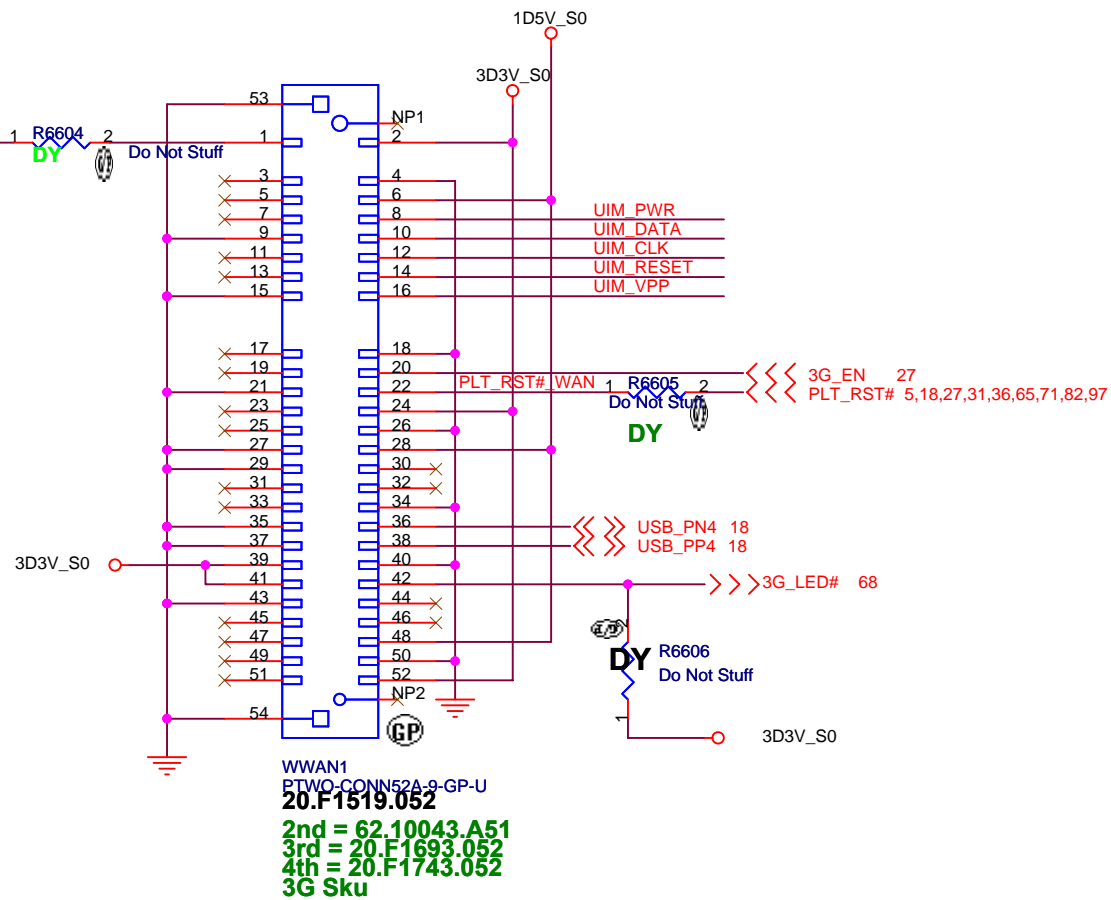
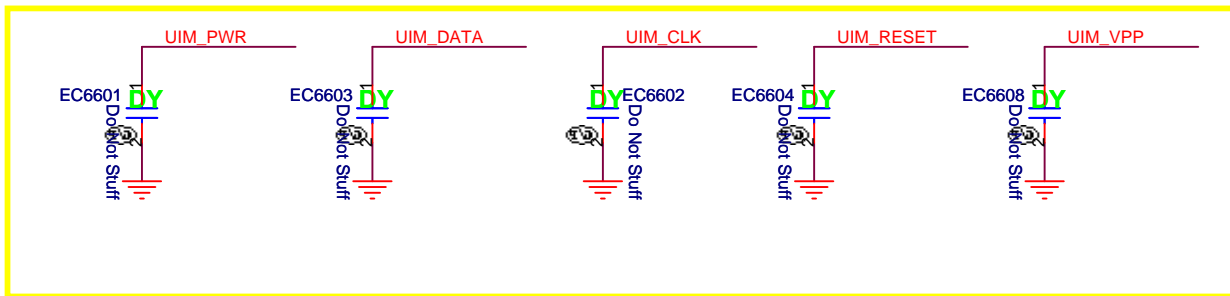
### ***Mini Card Connector(WWAN)***

20100712 V1.5

Place near MINI Card CONN



## RF suggestion



HR UMA

通資創緯

# Wistron Corporation

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Title

## WWAN Connector

Size

Document Number

# JE40-HR

Rev



Date: Thursday, December 02, 2010

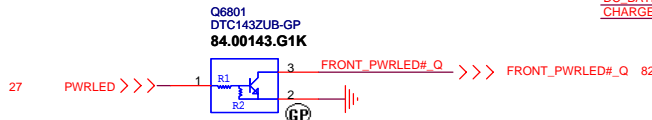
Sheet 66 of 102

( Blanking )

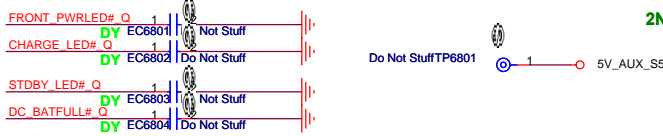
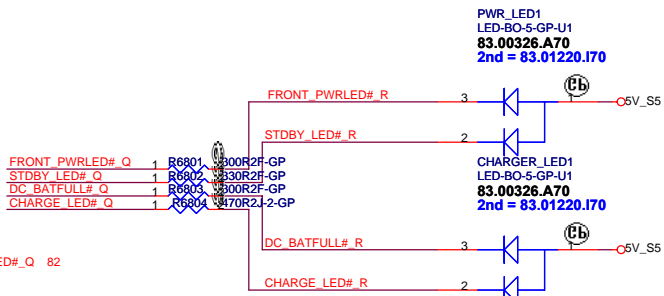
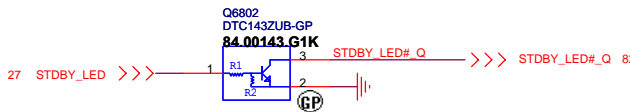
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 67 of 102

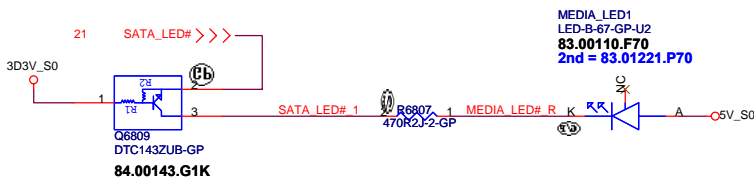
Power button LED



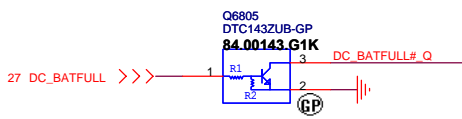
Power STDBY\_LED



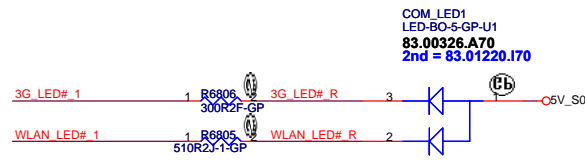
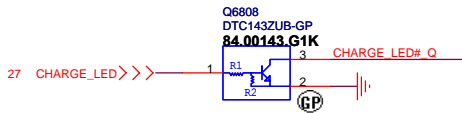
SATA HDD LED



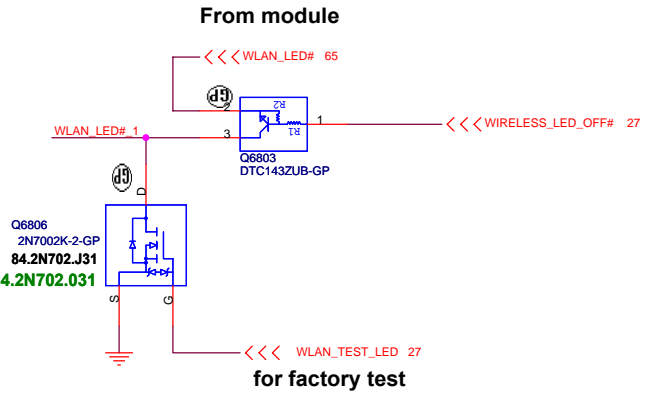
Battery LED2(DC\_BATFULL)



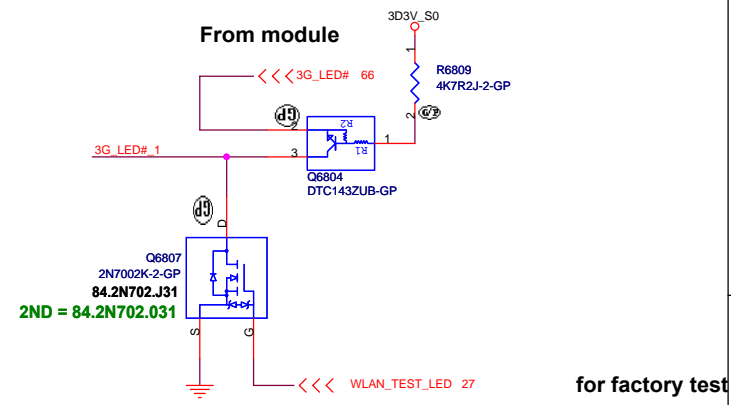
Battery LED1(CHARGE)



WLAN\_LED

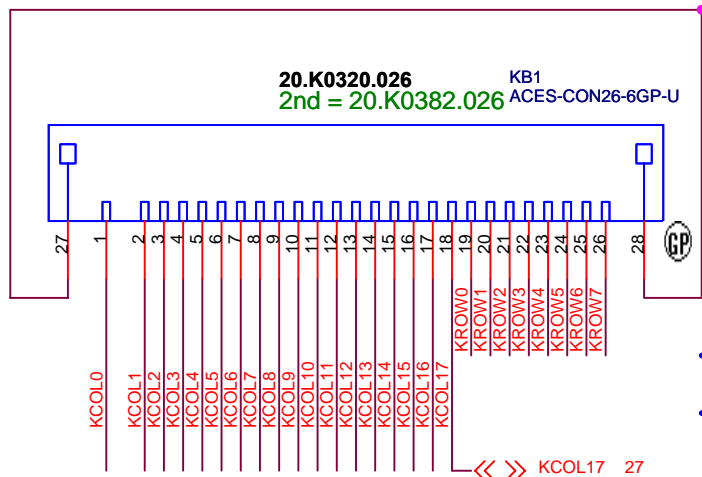


3G LED



SSID = KBC

## Internal KeyBoard Connector

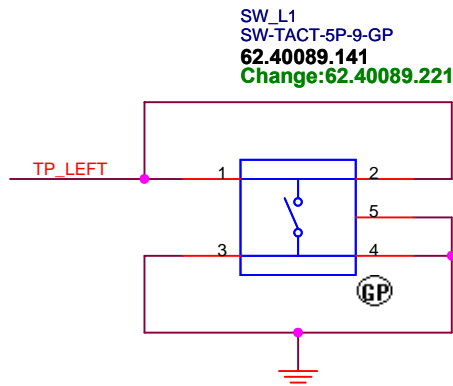
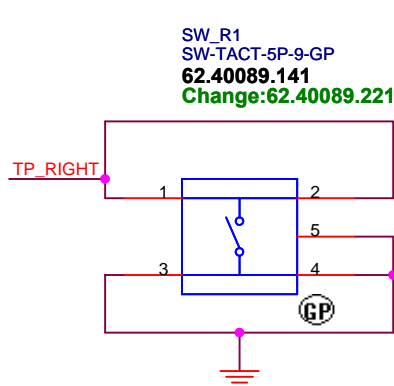


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

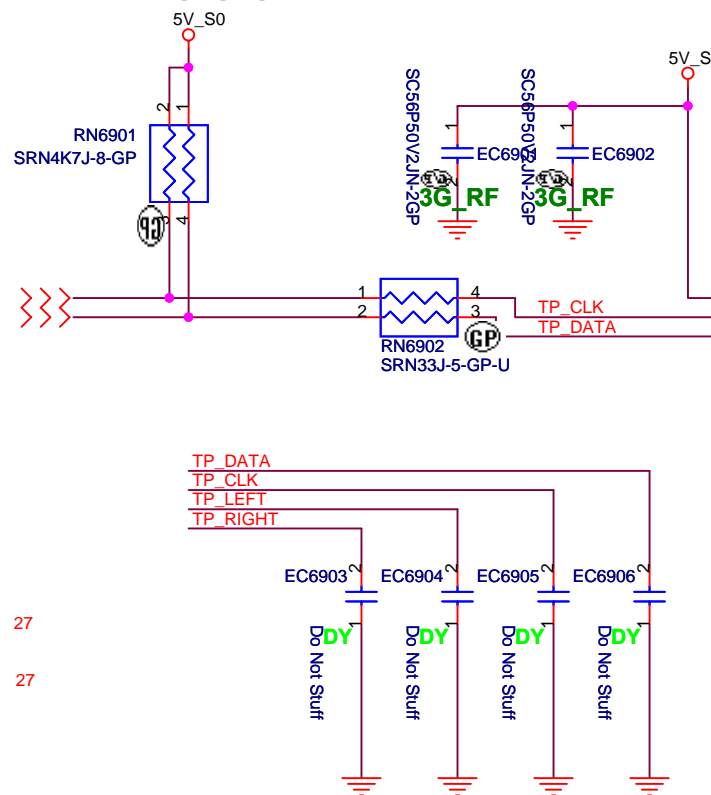
26

K/B

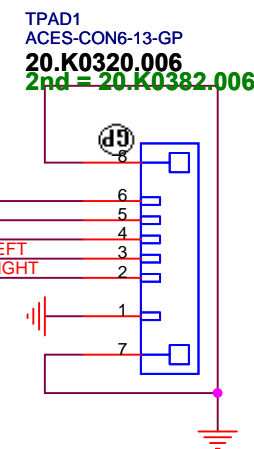
1 **SB to -1 modify Part number**



## TOUCH PAD



## FFC 異面



HR UMA

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Key Board/Touch Pad**

Size  
A4

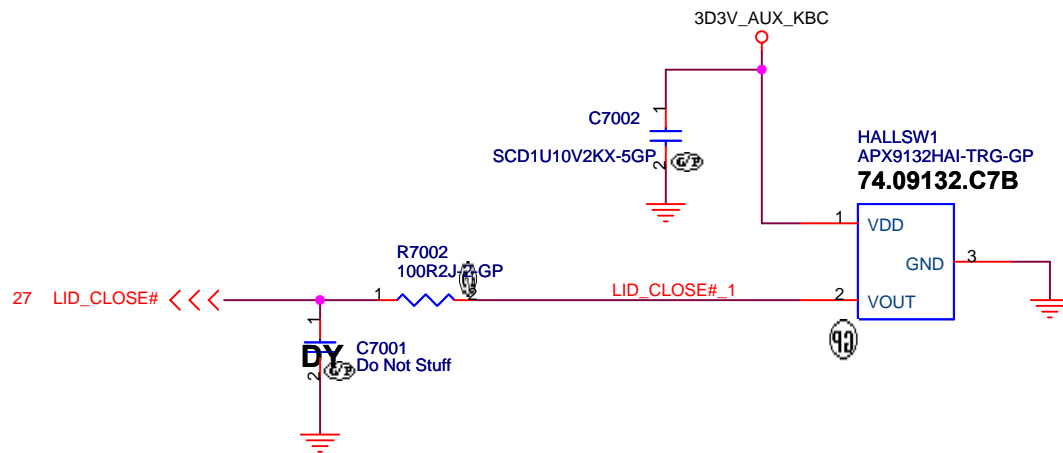
Document Number

**JE40-HR**

Rev  
-1

Date: Thursday, December 02, 2010

Sheet 69 of 102



HR UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size  
A4

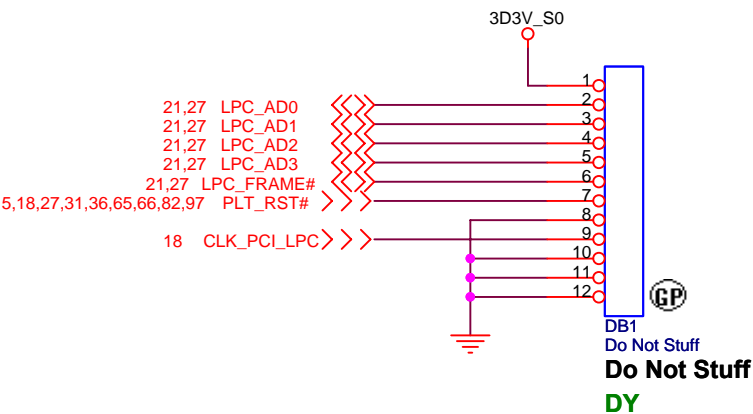
Document Number

**JE40-HR**

Rev  
**-1**

Date: Thursday, December 02, 2010

Sheet 70 of 102



HR UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Dubug connector</b>			
Size A4	Document Number <b>JE40-HR</b>		Rev <b>-1</b>
Date: Thursday, December 02, 2010		Sheet 71 of	102

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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
JE40-HR

Date: Thursday, December 02, 2010

Reserved

Rev  
-1

Sheet 72 of 102



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**JE40-HR**

Date: Thursday, December 02, 2010

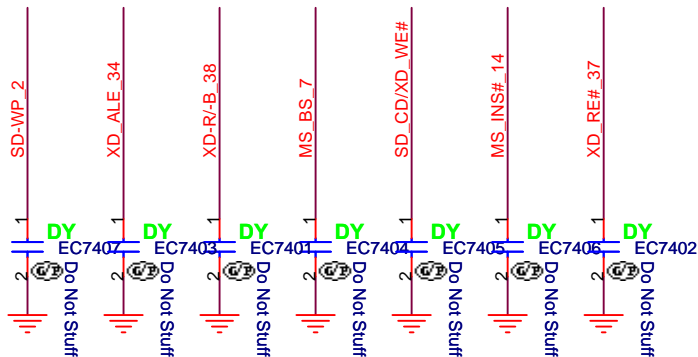
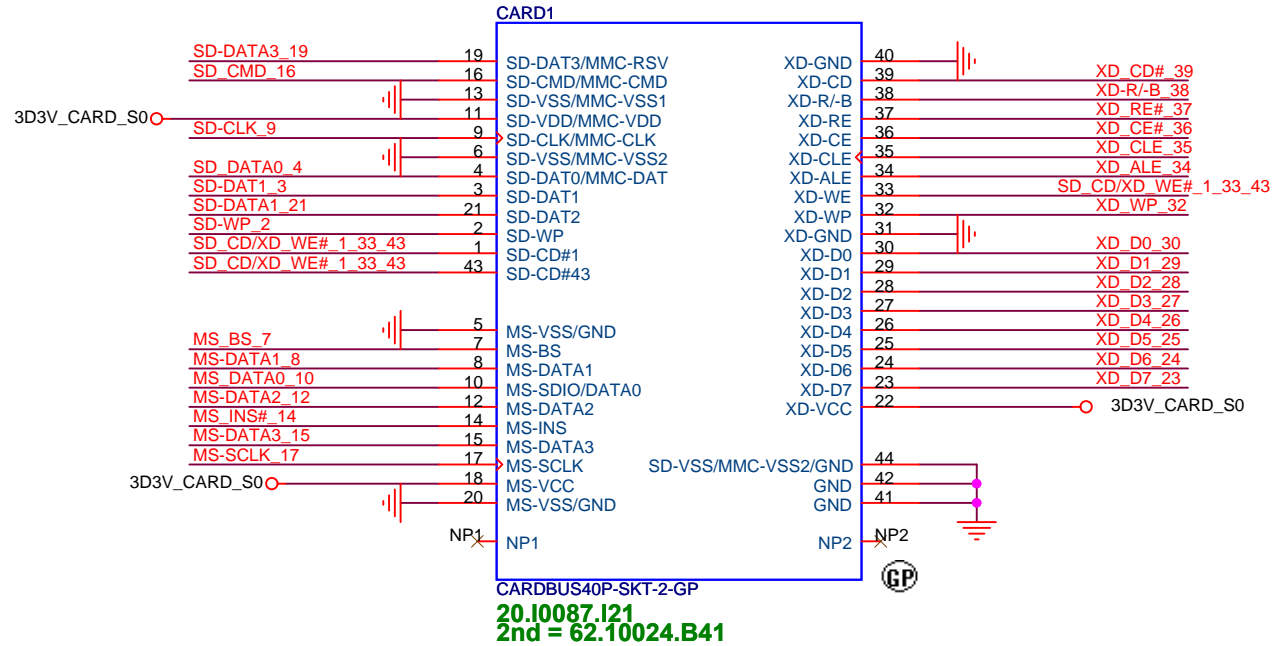
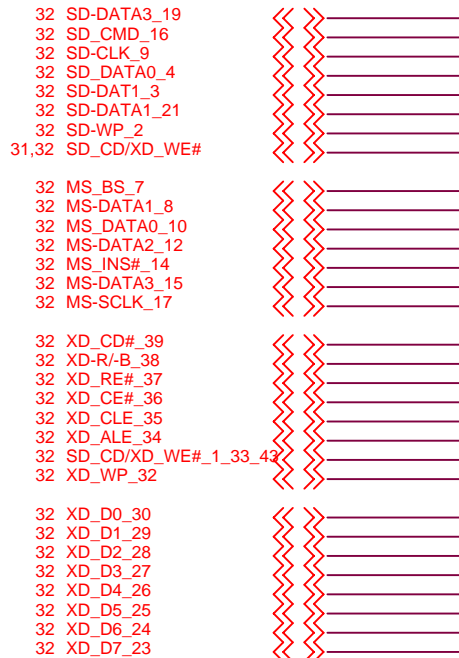
Reserved

Rev  
**-1**

Sheet 73 of 102

SSID = SDIO

# SD/XD/MS Card Reader



HR UMA

緯創資通

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Title

CARD Reader CONN

Size

Document Number

Rev

JE40-HR

-1

Date: Thursday, December 02, 2010

Sheet 74 of 102

SSID = ExpressCard

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA

(Blanking)

HR UMA

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 76 of 102



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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 78 of 102

SSID = User.Interface

## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

### Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

HR UMA

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Free Fall Sensor**

Size  
A4

Document Number

**JE40-HR**

Rev  
**-1**

Date: Thursday, December 02, 2010

Sheet 79 of 102

( Blanking )

HR UMA

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 80 of 102

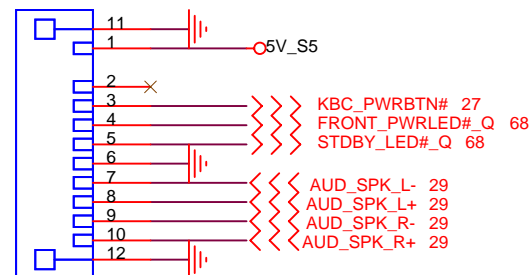


( Blanking )

HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 81 of 102

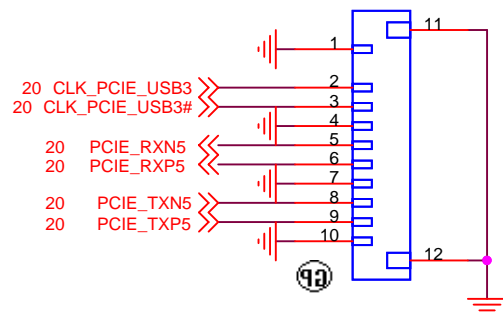
## PWRCN1 FFC 異面



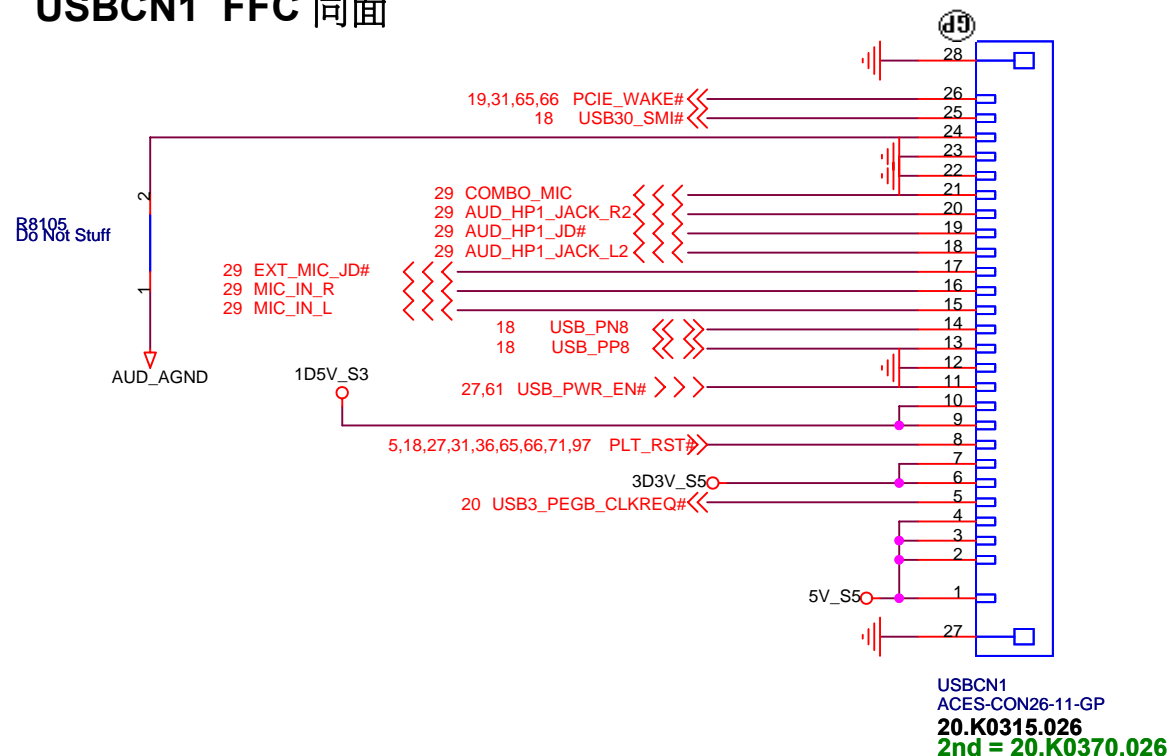
PWRCN1  
ACES-CON10-20-GP  
**20.K0422.010**  
2nd = 20.K0382.010

## 0806 change 10Pin

USBCN2  
ACES-CON10-18-GP  
**20.K0315.010**  
2nd = 20.K0392.010

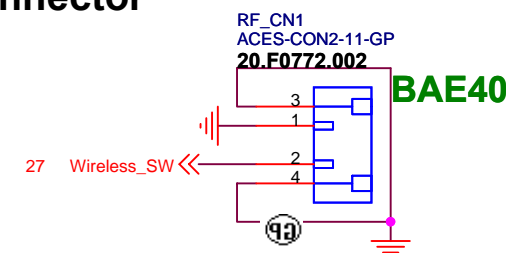


## USBCN1 FFC 同面



## USBCN2 FFC 同面

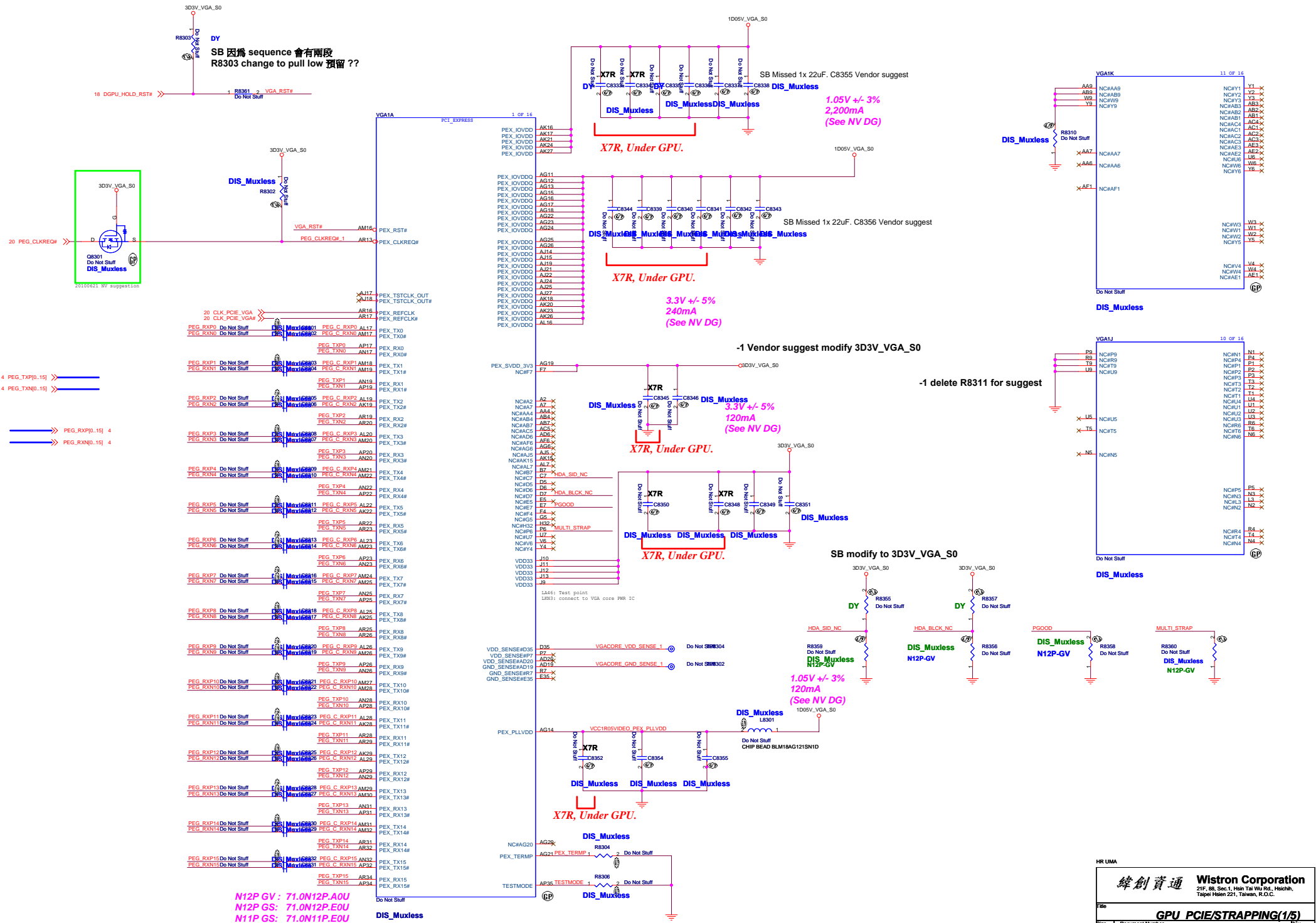
-1 add RF connector  
BAE40 Only



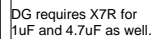
## Cabele Wire to BD

HR UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
<b>IO Board Connector</b>		Size A4	
<b>JE40-HR</b>		Document Number	
Date: Thursday, December 02, 2010		Rev -1	
Sheet 82 of 102		Page 1 of 1	

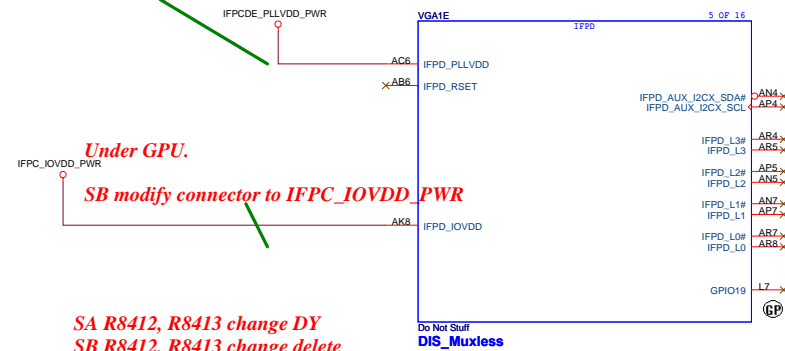


VGA1G		IFPB	7 OF 16
			IFPA_TXD0# IFPA_TXD0
			IFPA_TXD1# IFPA_TXD1
0	IFPB_PLLVDD		IFPA_TXD2# IFPA_TXD2
1	IFPB_RSET		IFPA_TXD3# IFPA_TXD3
			IFPA_TXC# IFPA_TXC
			IFPB_TXD4# IFPB_TXD4
0	IFPA_OVDD		IFPB_TXD5# IFPB_TXD5
0	IFPB_OVDD		IFPB_TXD6# IFPB_TXD6
			IFPB_TXD7# IFPB_TXD7
			IFPB_TXC# IFPB_TXC
			GPI00



*X7R, Under GPU.*

***SB modify connector to IFPCDE\_PLLVDD\_PWR***



*Under GPU.*

*SB modify connector to IFPC\_IOVDD\_PWR*

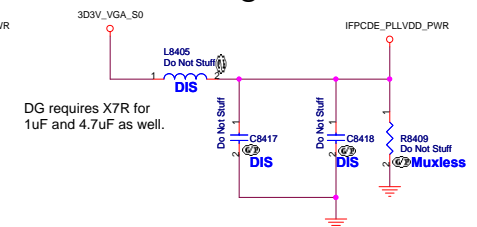
**SA R8412, R8413 change DY**  
**SB R8412, R8413 change delete**



1.05V +/- 3%  
285mA  
(See NV DG) 220ohm@100MHz ESR=0.05  
1D05V\_VGA\_S0

*X7R, Under GPU.*

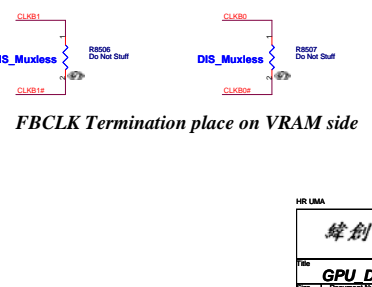
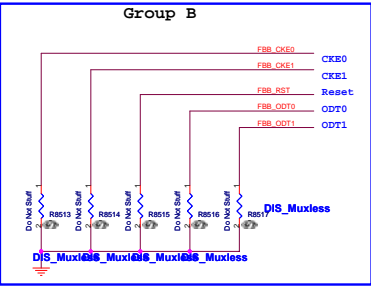
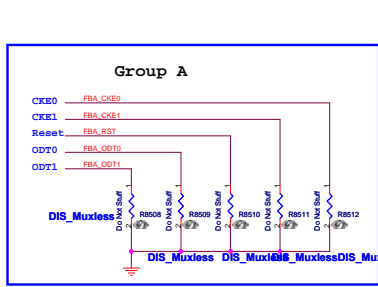
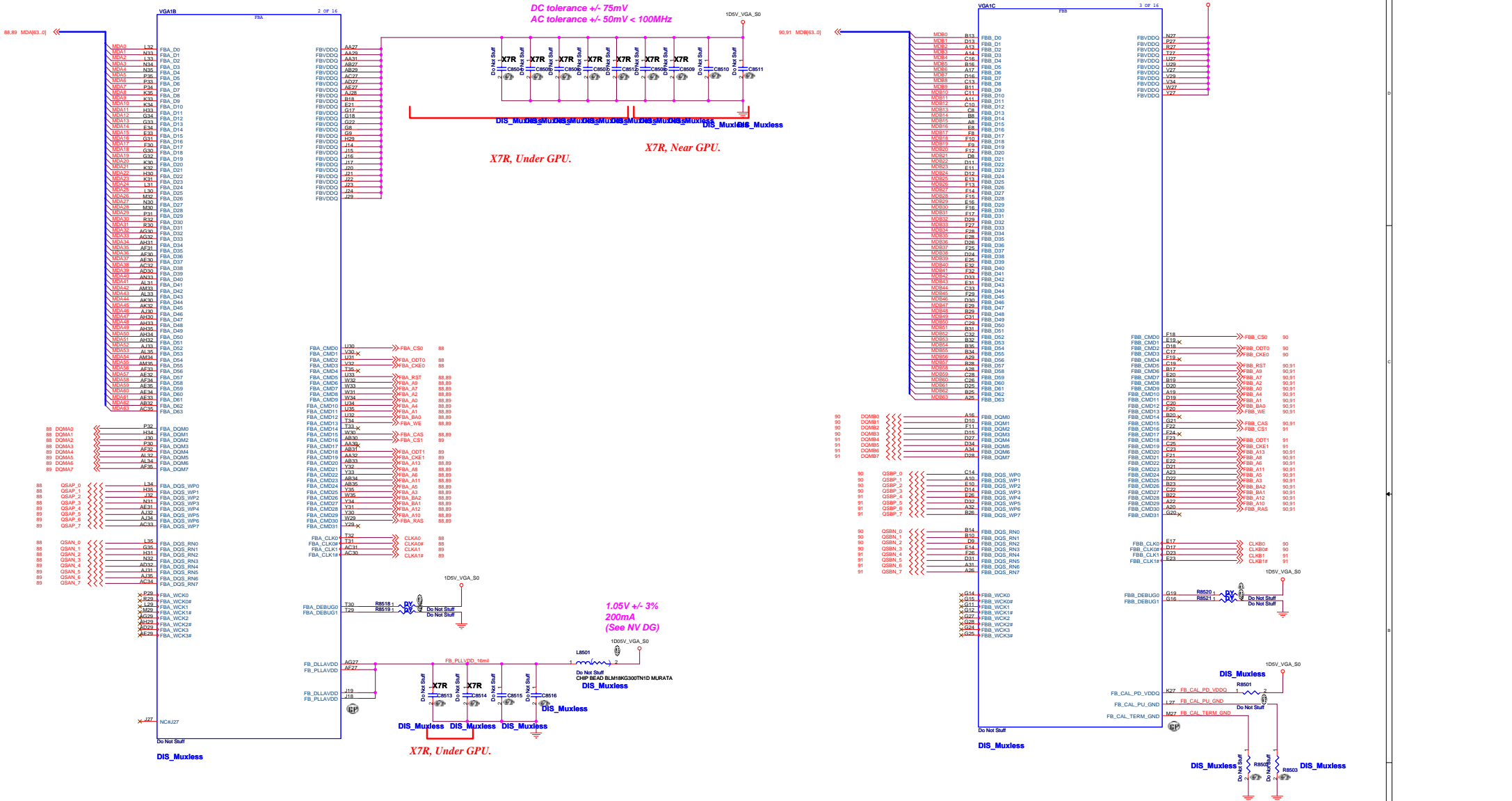
3.3V +/- 5%  
440mA (220mA each, max 2 links)  
(See NV DG) 300ohm@100MHz ESR=0.25



DG requires X7R for 1uF and 4.7uF as well.

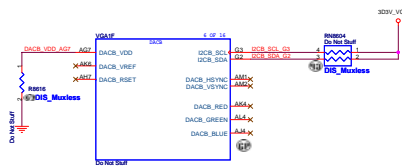
# EDP 10A

DC tolerance +/- 75mV  
AC tolerance +/- 50mV < 100MHz

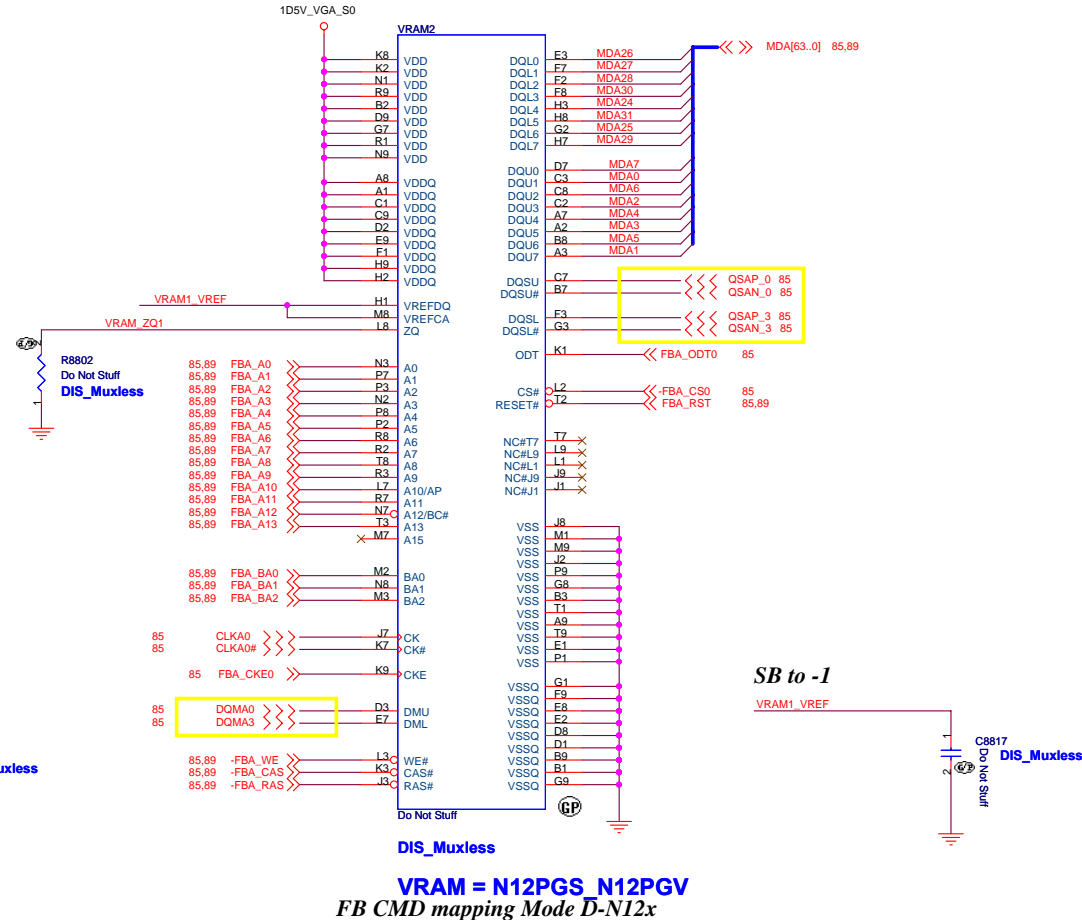
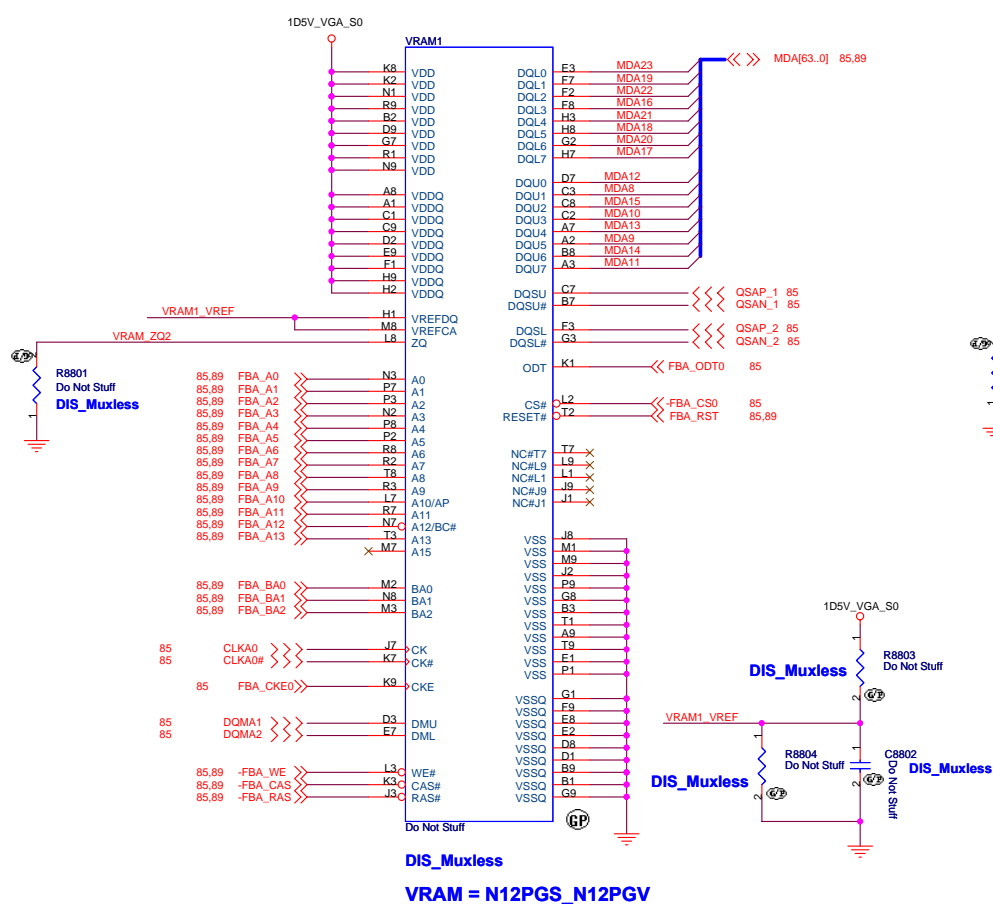


FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

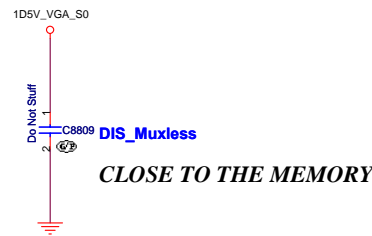
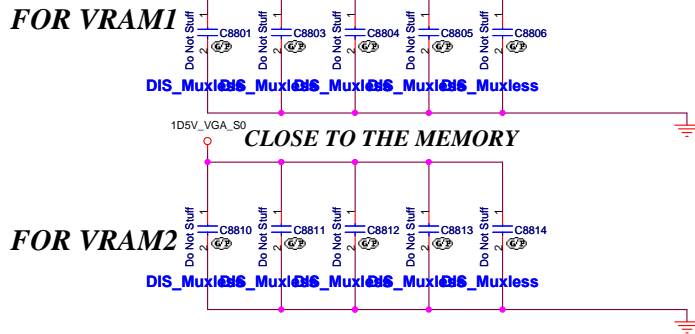




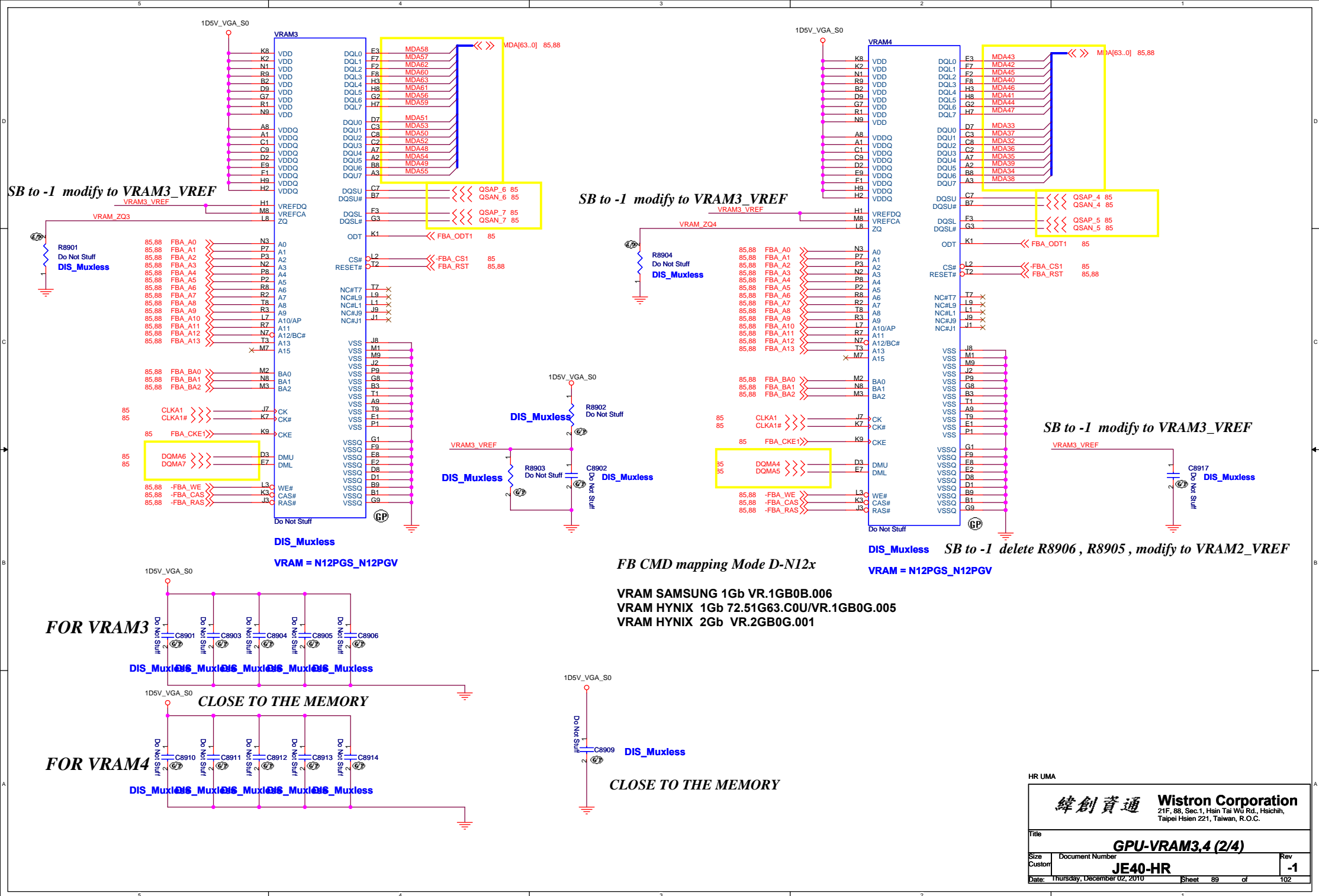


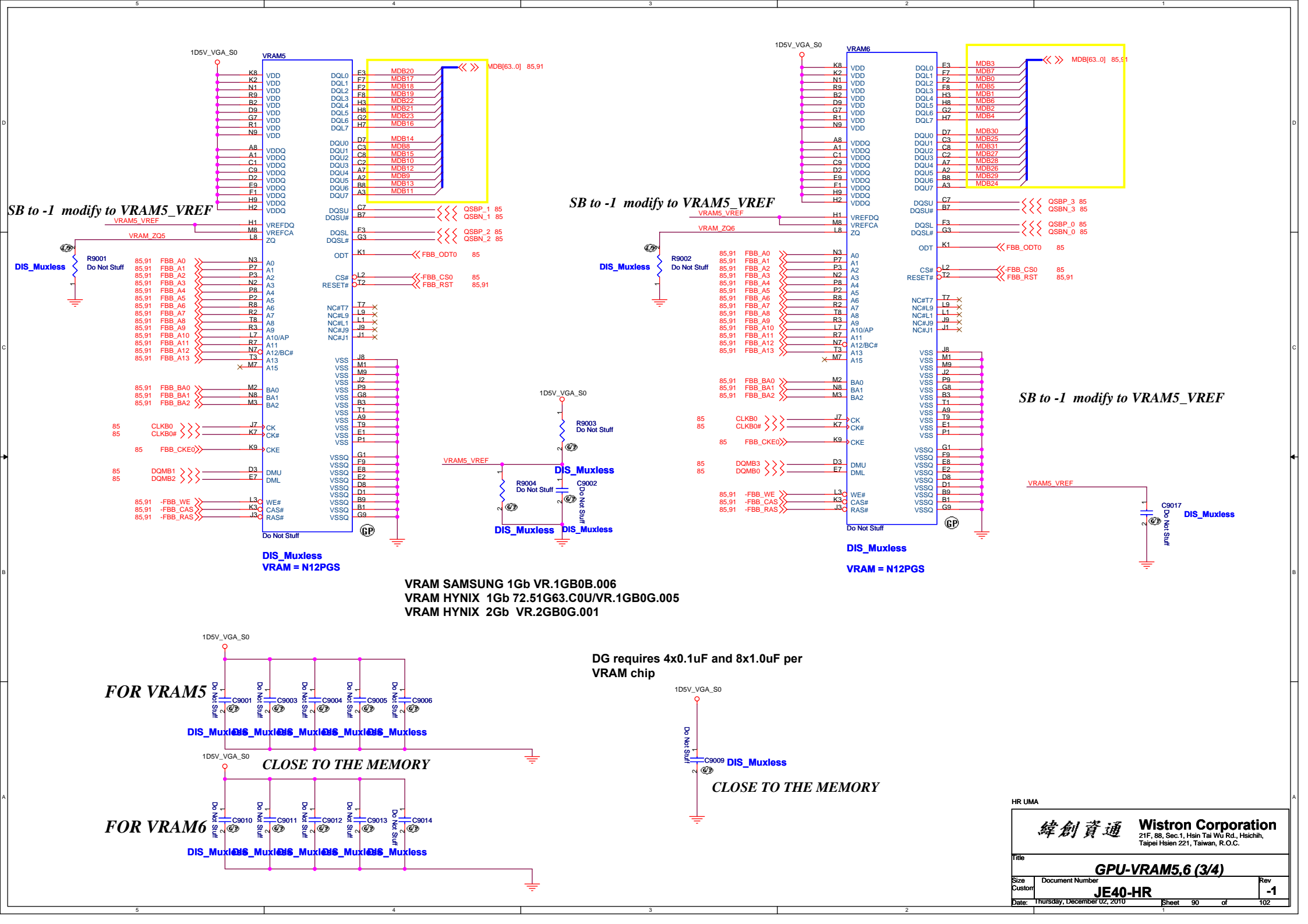
VRAM SAMSUNG 1Gb VR.1GB0B.006  
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
 VRAM HYNIX 2Gb VR.2GB0G.001

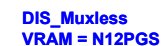
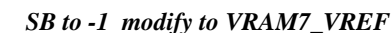
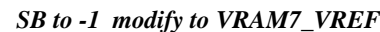
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



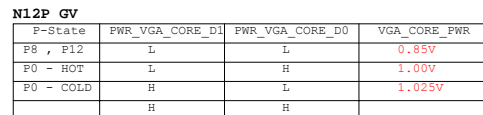




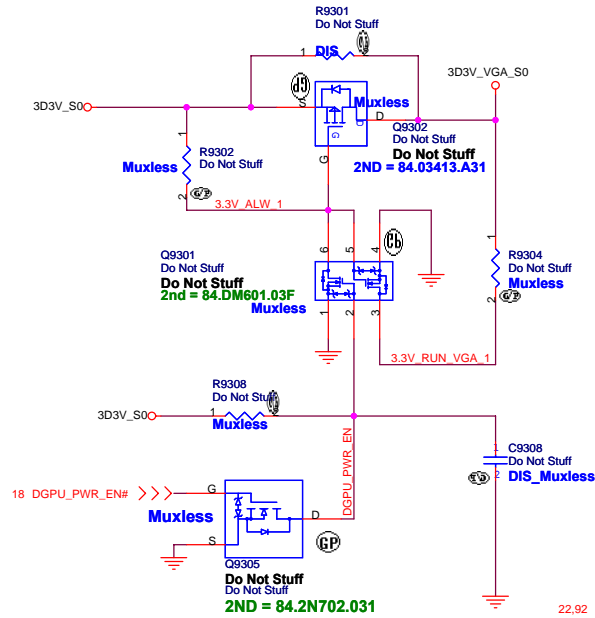




VRAM SAMSUNG 1Gb VR.1GB0B.006  
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
VRAM HYNIX 2Gb VR.2GB0G.001


$$V_{out} = 0.75V * (R1 + R2) / R2$$

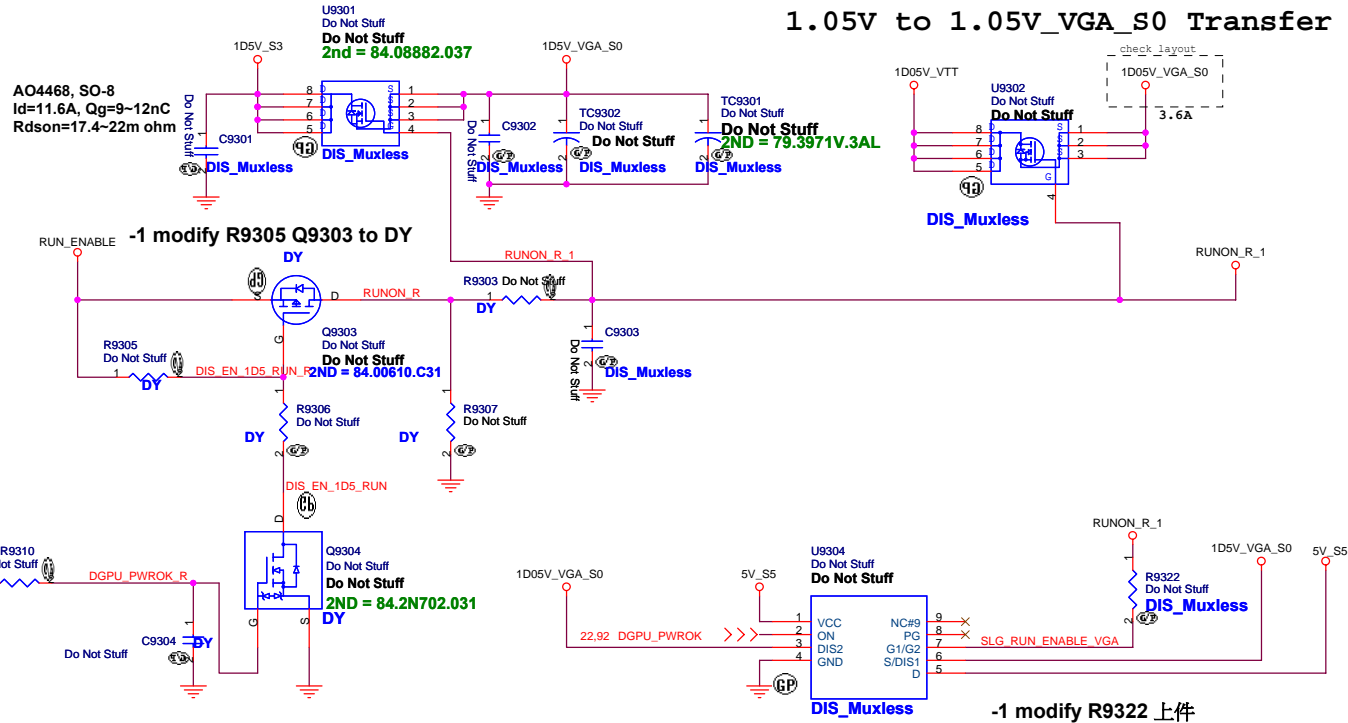
## +3VS to 3.3V\_DELAY Transfer



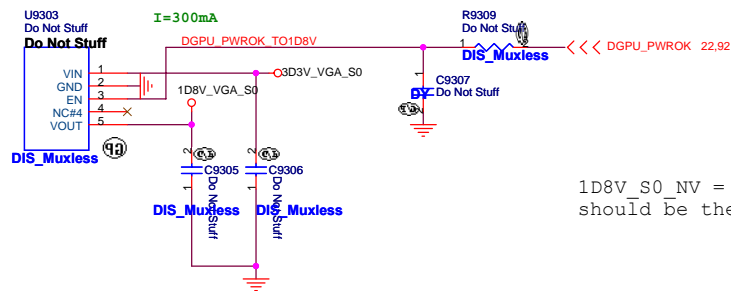
## 1D5V\_VGA\_S0

SB modify to 84.03006.A37

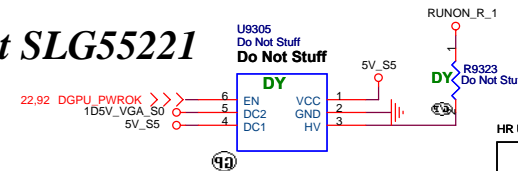
## 1.05V to 1.05V\_VGA\_S0 Transfer



## RT9025 for 1D8V\_VGA +3VS to 1.8V Transfer

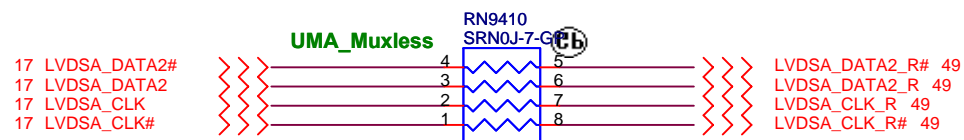
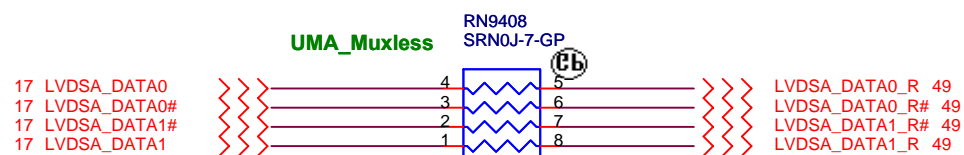
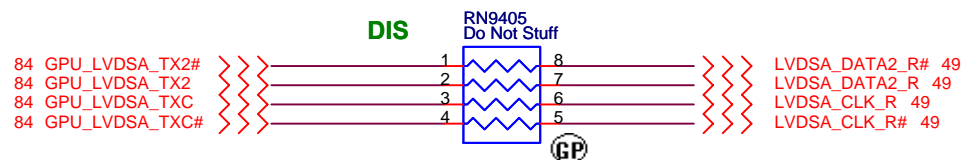
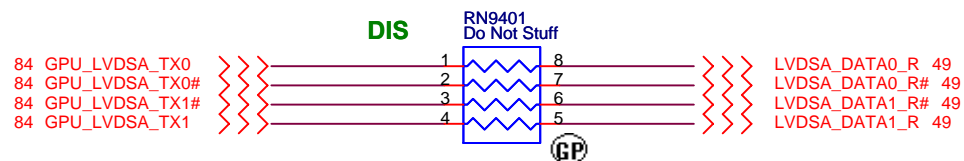


## -1 co-layout SLG55221

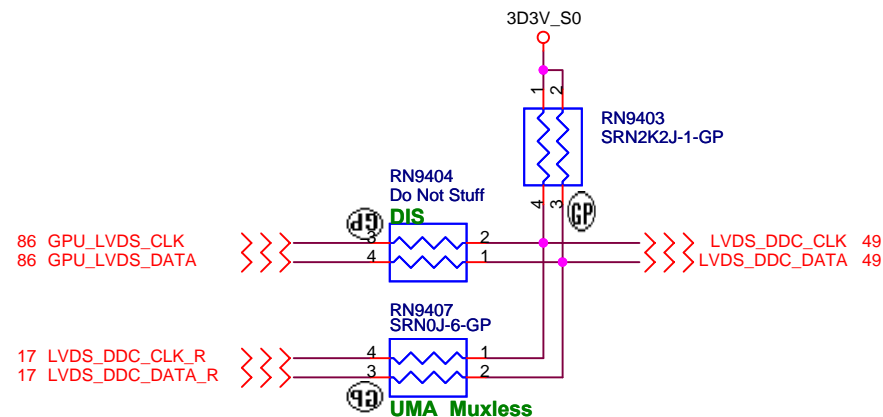
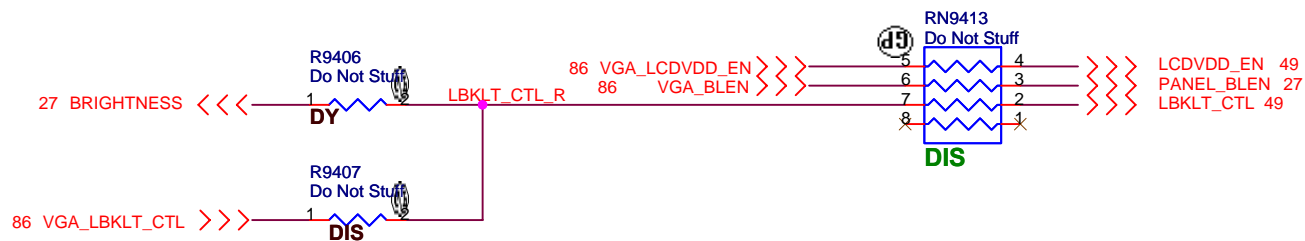
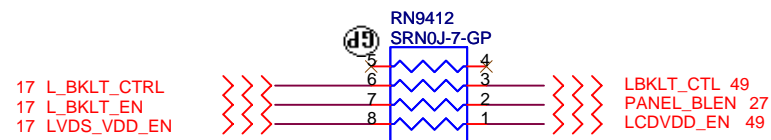


<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>DISCRETE VGA POWER</b>	
Size Custom	Document Number <b>JE40-HR</b>
Date: Thursday, December 02, 2010	Rev <b>-1</b>
Sheet 93 of 102	1

# LVDS Channel A



## Panel BL brightness/Power En/BL En



HR UMA

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**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**LVDS Switch**

Size

Document Number

**JE40-HR**

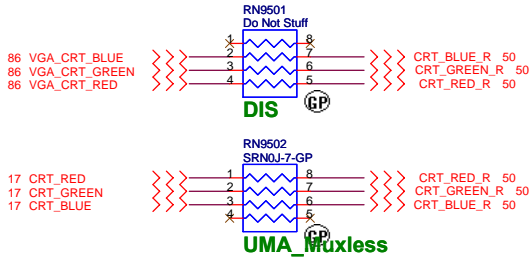
Rev

**-1**

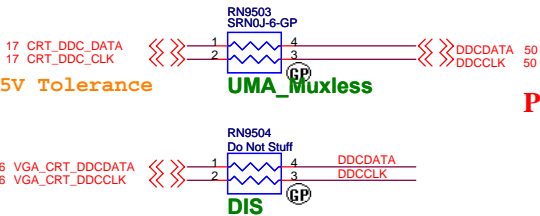
Date: Thursday, December 02, 2010

Sheet 94 of 102

Close to CRT Board CONN

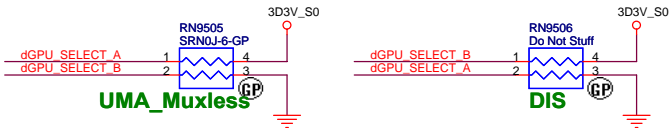


CRT DDCDATA & DDCCLK



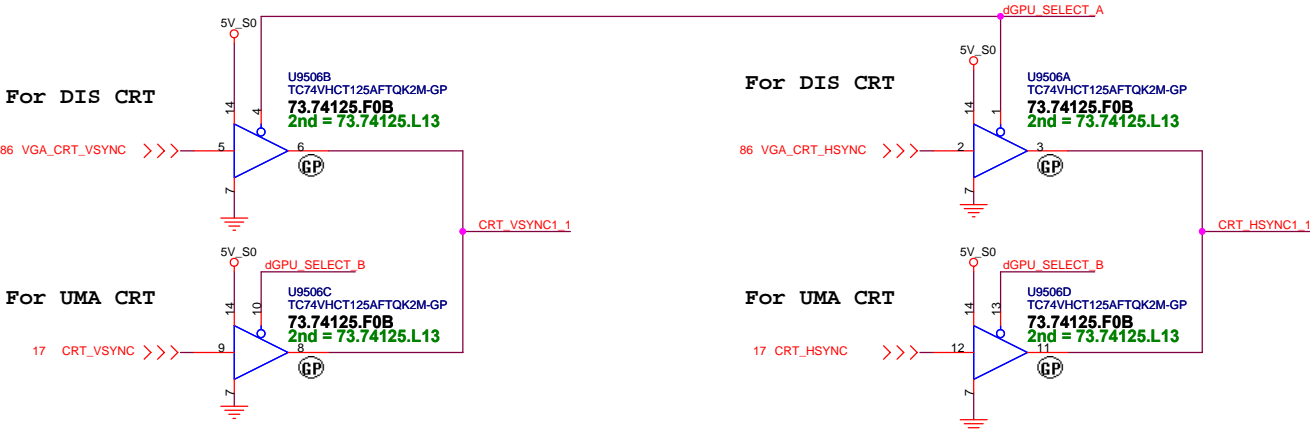
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS  
H=>B1 -UMA

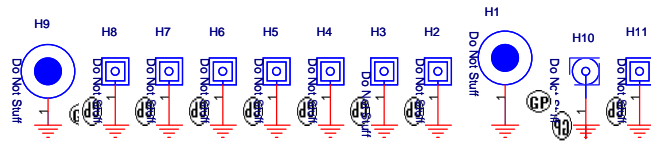


SB to -1 modify R9503,R9504 to 10 ohm



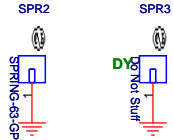
SSID = SDIO



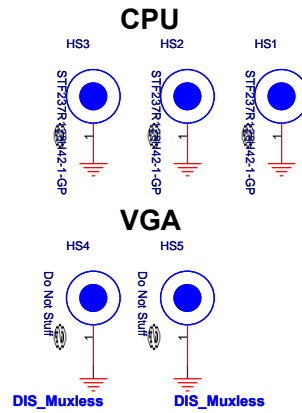
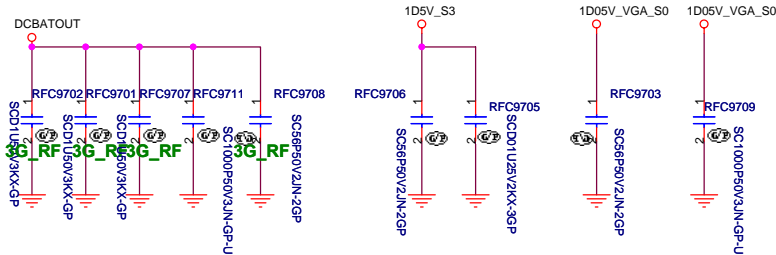
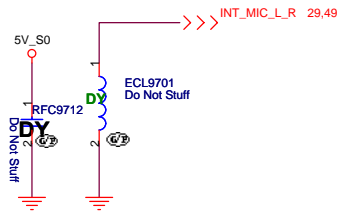
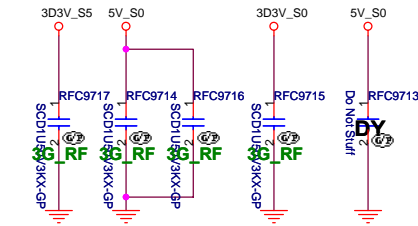


SB to -1 BOM add SPR2

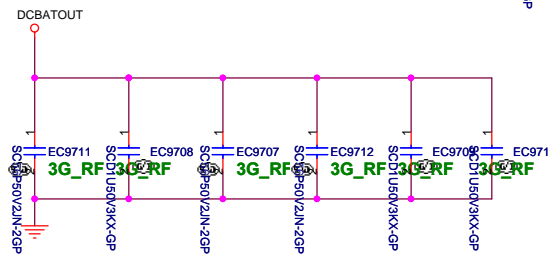
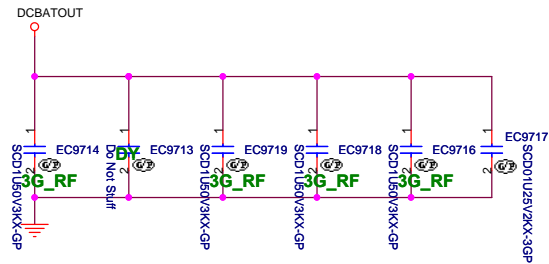
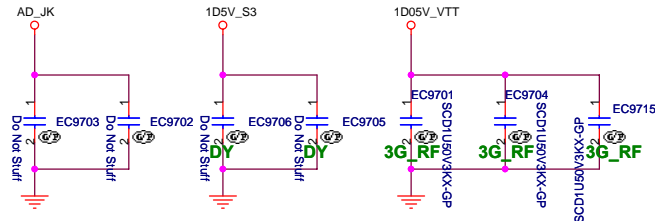
-2 delete SPR5



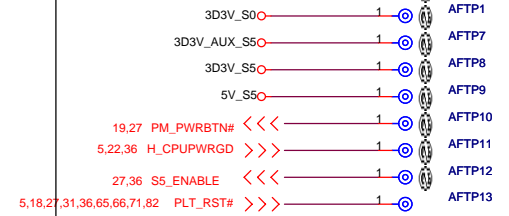
Change:34.40V16.001



3G Sku



Check test point



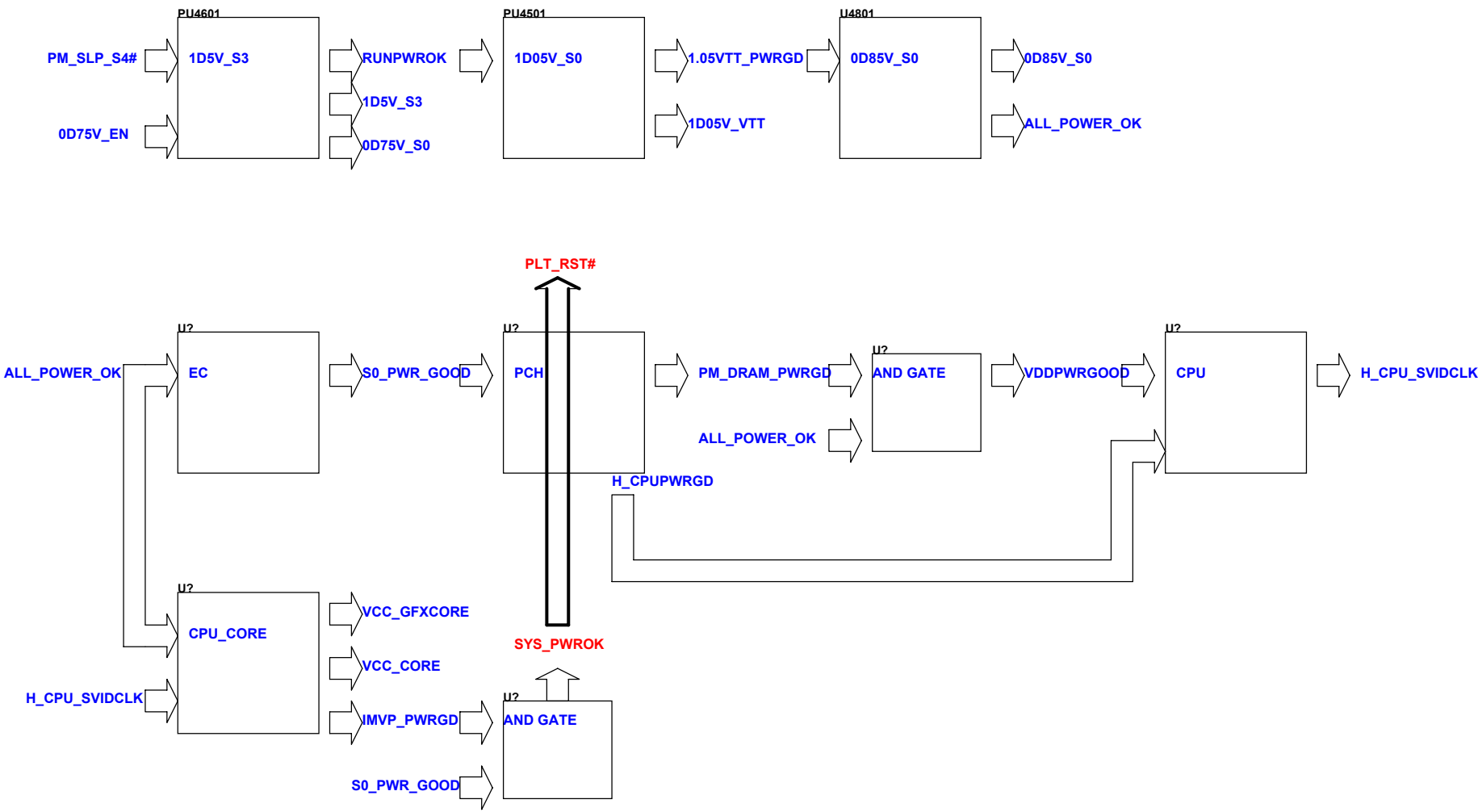
Test Point放在Dimm Door打開可量測處

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>UNUSED PARTS/EMI Capacitors</b>		
Size A3	Document Number <b>JE40-HR</b>	Rev <b>-1</b>
Date: Thursday, December 02, 2010	Sheet 97 of 102	

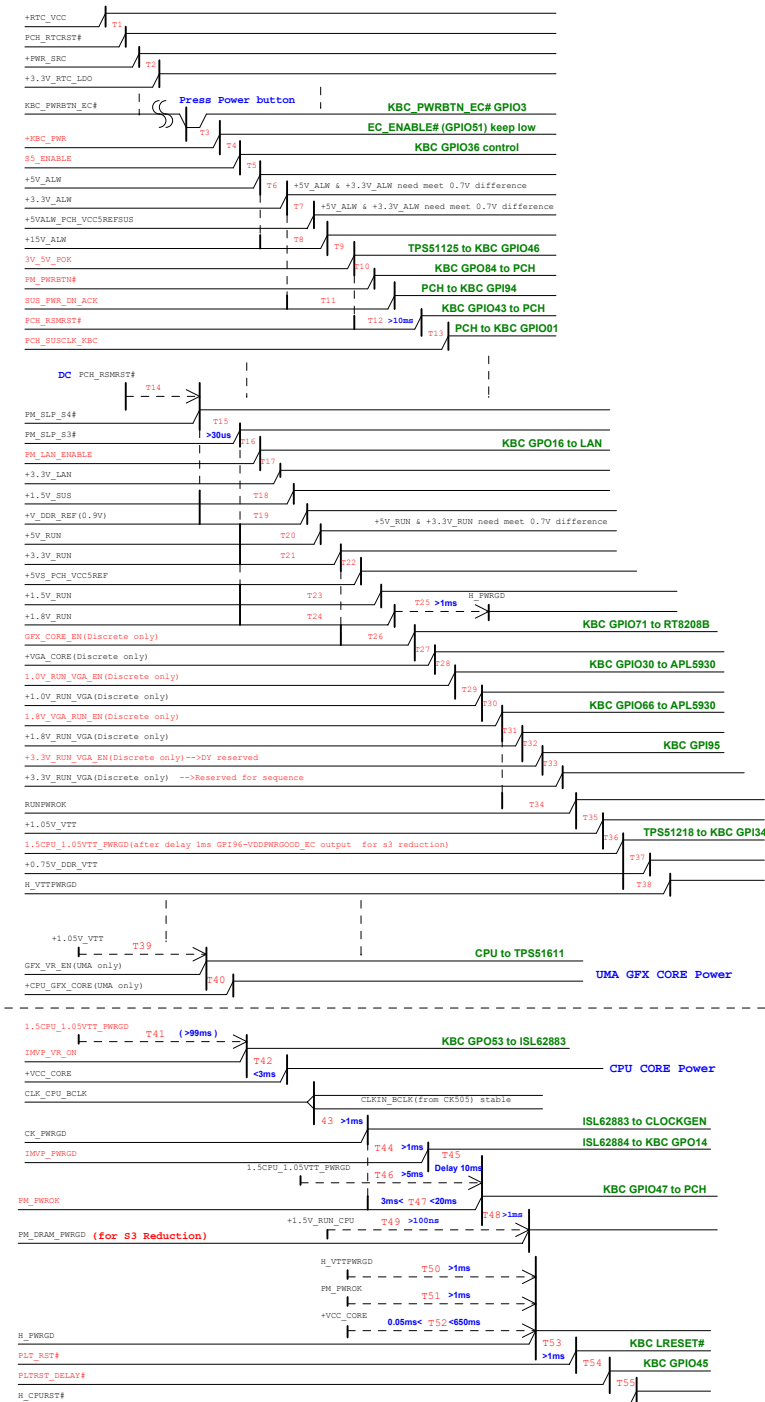
Power Sequence

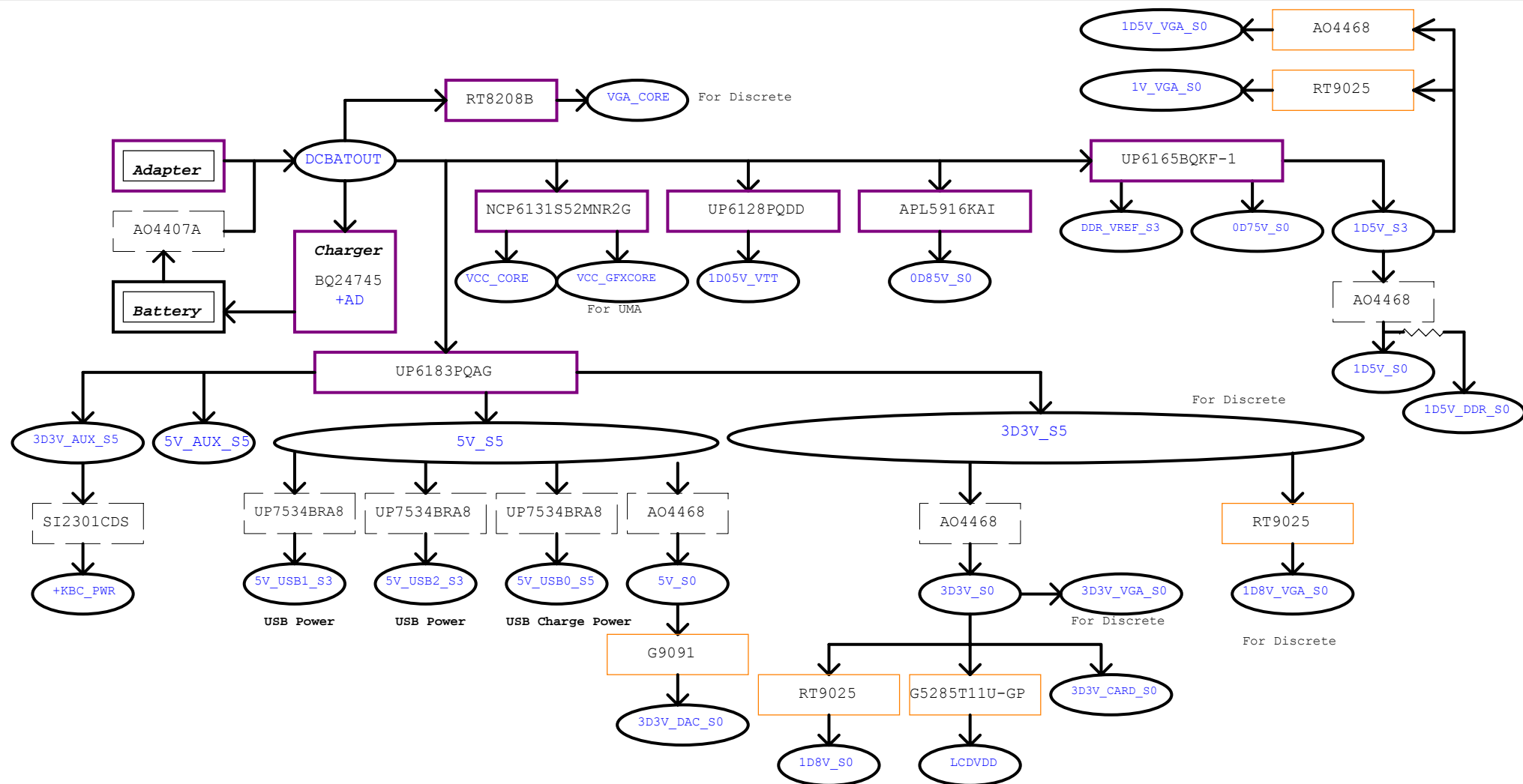


(AC mode)

[illegible]

red word: KBC GPIO





### Power Shape



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

### ***Power Block Diagram***

Size

Document Number

**JE40-HR**

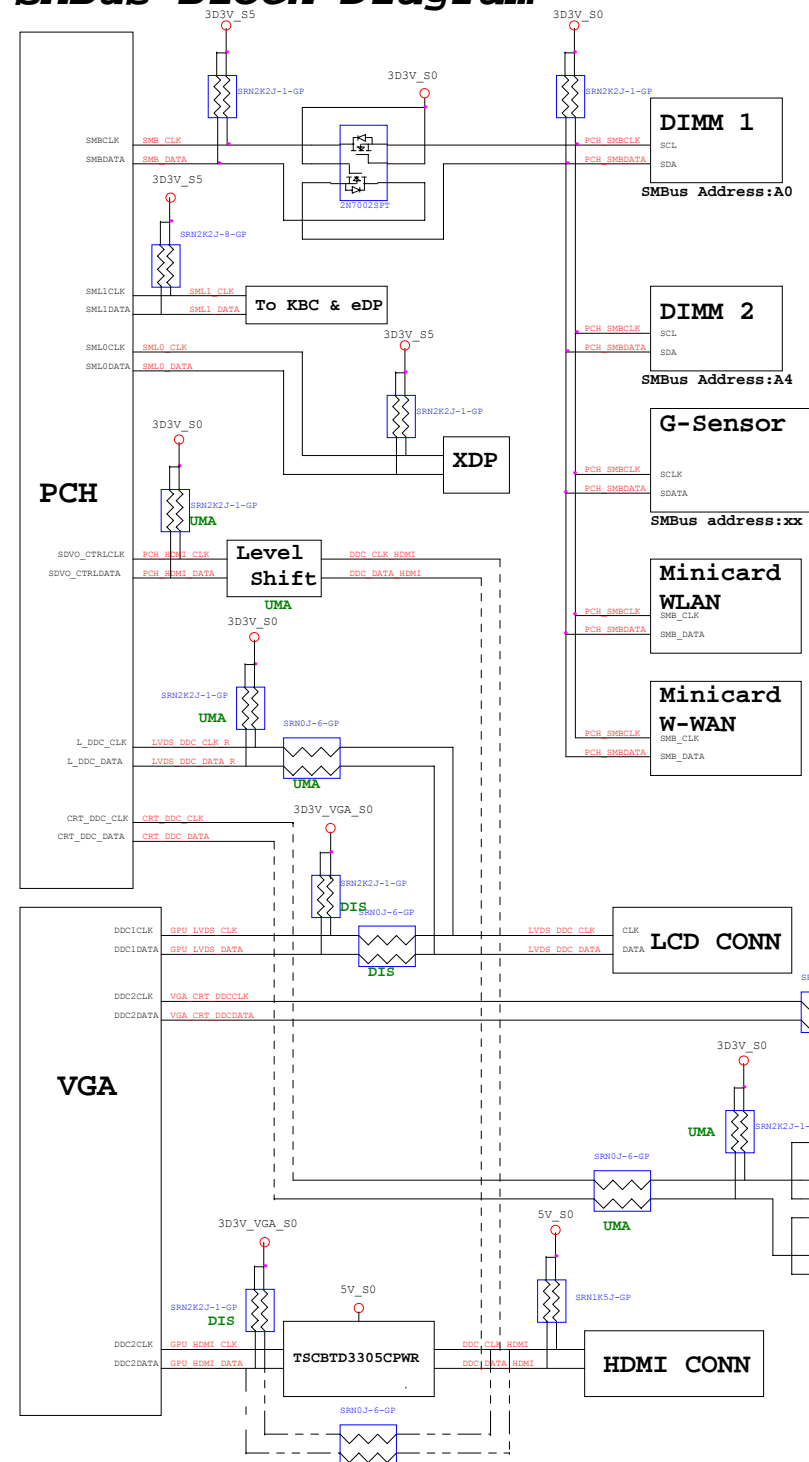
Rev

**-1**

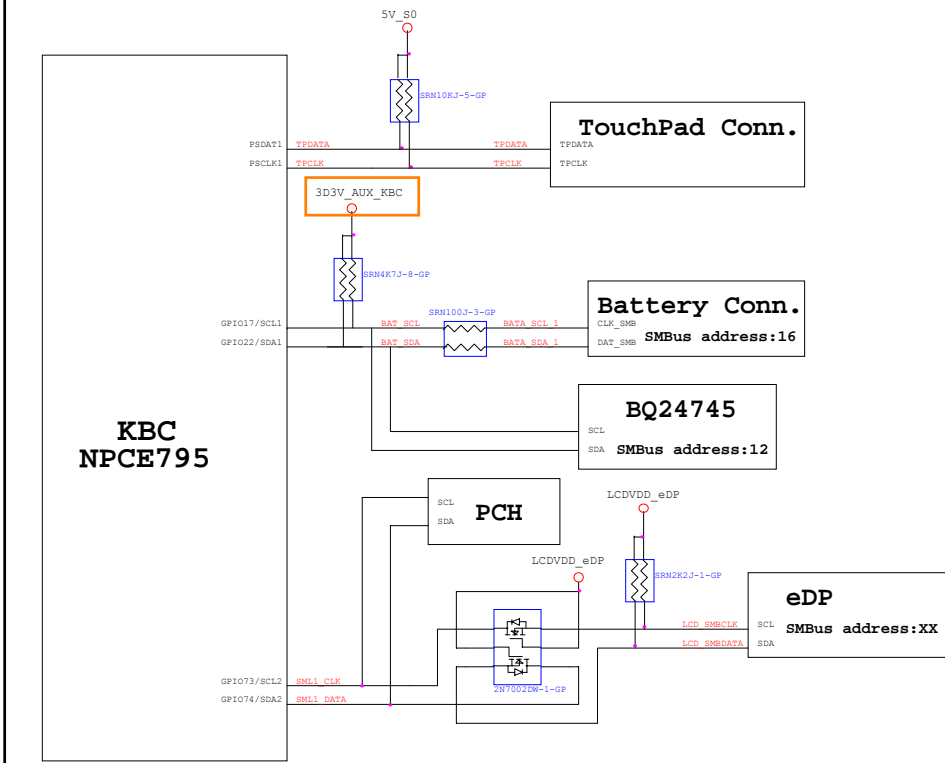
Date: Thursday, December 02, 2010

Sheet 100 of 102

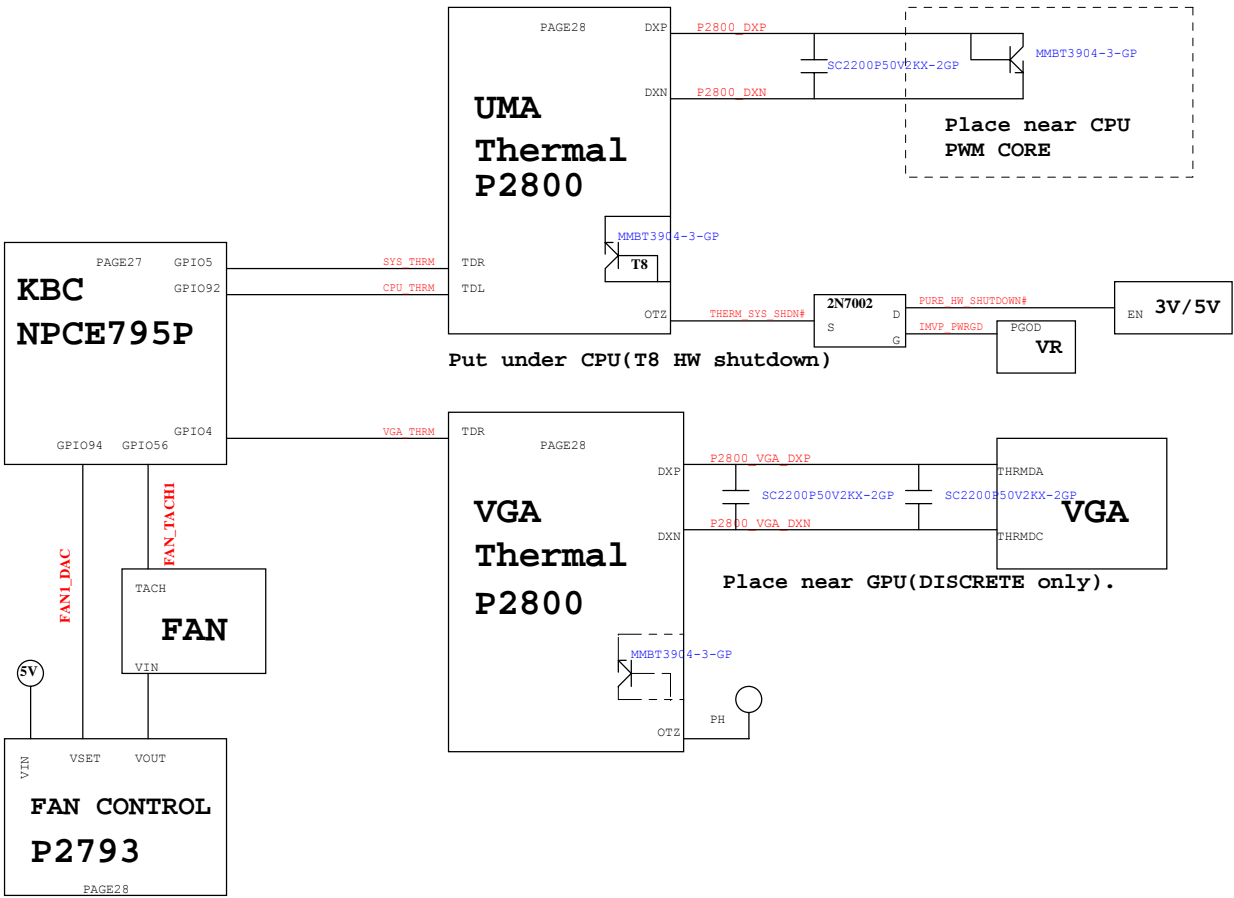
PCH SMBus Block Diagram



KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram

