

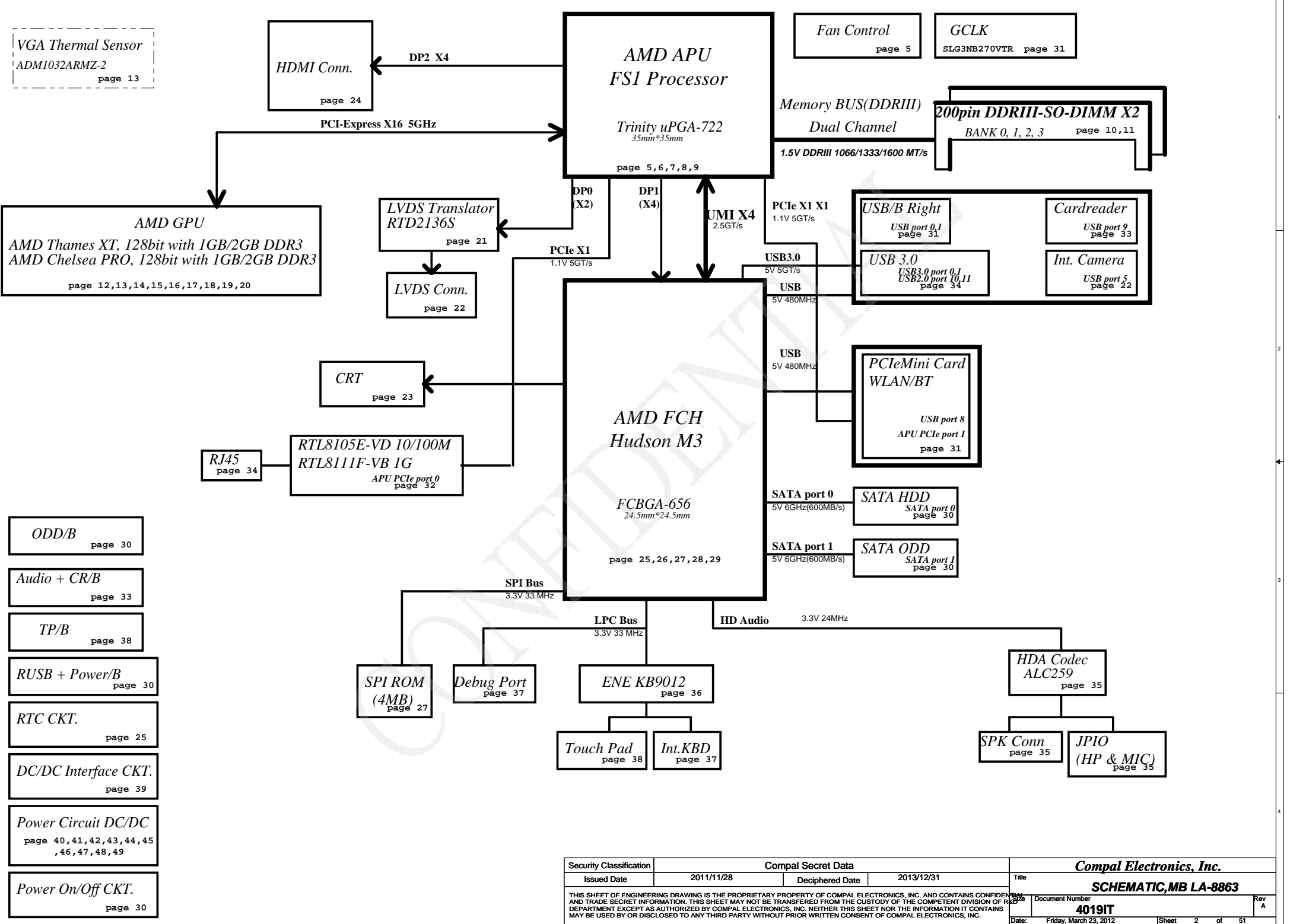
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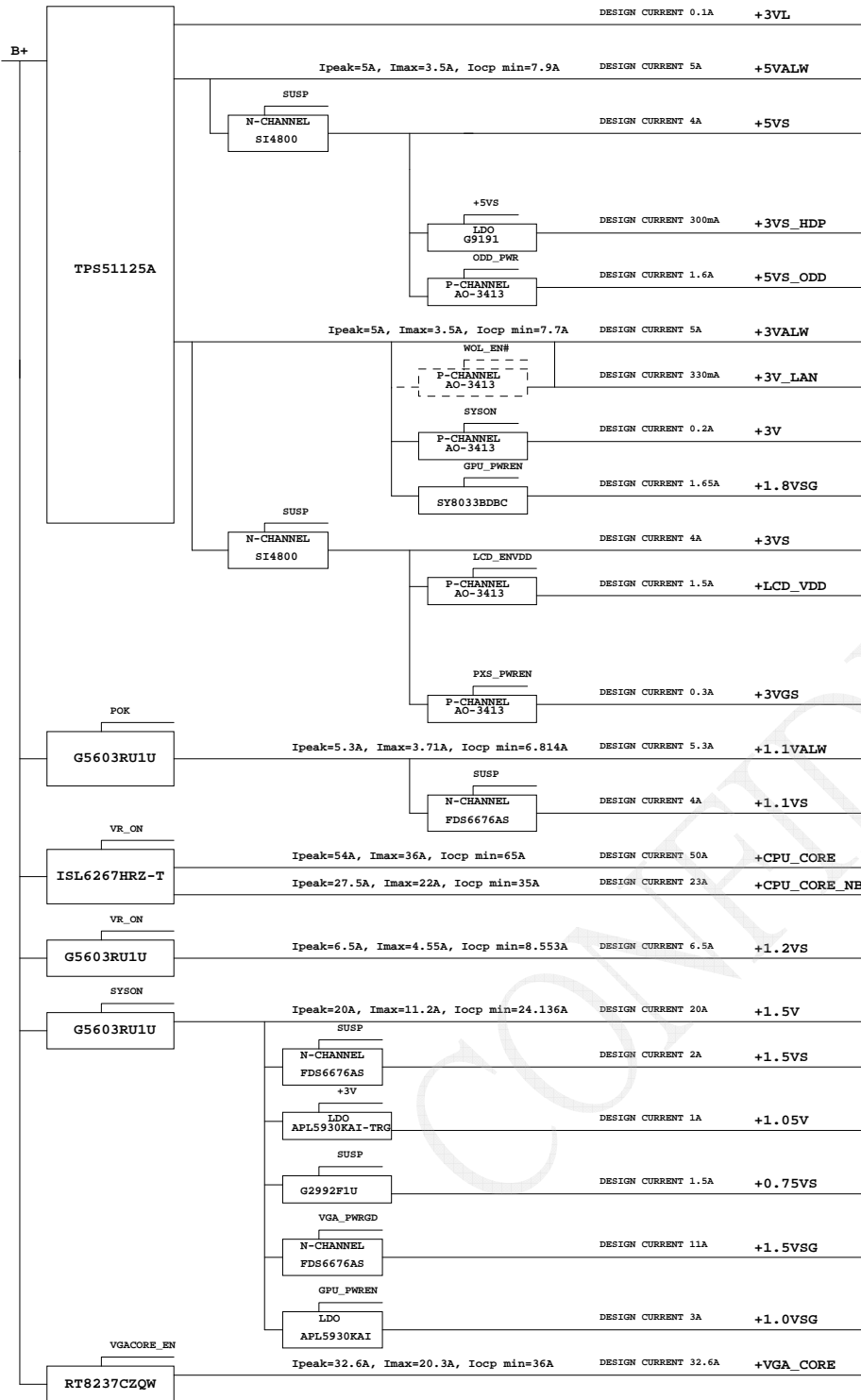
Eureka Discrete

LA-8863P REV 0.3 Schematic

AMD Trinity APU / Hudson M3 FCH
Thames XT & Chelsea PRO
2012-03-13 Rev 0.3

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/28	Deciphered Date	2013/12/31	Title	SCHEMATIC,MB LA-8863
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				Rev	A

Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VGS +1.8VSG +1.5VSG +1.0VSG
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress		COMMON		UMA	PowerXpress	Discrete
BTO	IHDMI@		HDMI@		UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function	MINI PCI-E SLOT	LAN				
description		LAN				
explain		10/100M		GIGA		
BTO		8105ELDO@	8105ESWR@	8111E@		

Function		Cam & Mic	Panel			
description		Cam & Mic	Panel (DIS@)			
explain		Cam & Mic				
BTO		CAM@				

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		FCH			
description	PowerXpress		FCH			
explain	BACO mode	Non-BACO	Hudson-M2	Hudson-M3		
BTO	BACO@	NOBACO@	M2@	M3@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	90 H	1001 000xb
+3VS	DDR SO-DIMM 1	92 H	1001 001xb
+3VS	WLAN		

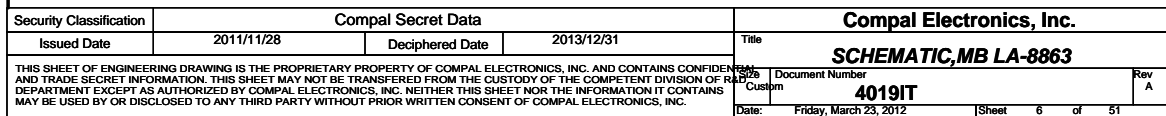
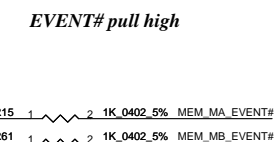
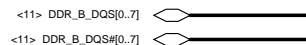
EC SM Bus1 Address

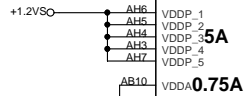
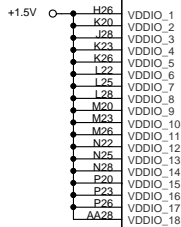
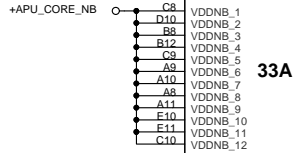
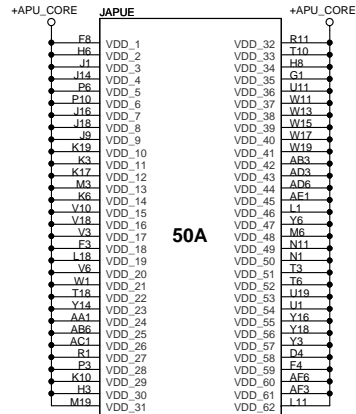
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011x b
+3VL	Charger IC	12 H	0001 001x b
EC SM Bus3 Address			
+3VS	LVDS EEPROM	A8 H	1010 1000 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	APU Thermal Sensor	98 H	1001 100x b
+3VS	GPU Internal Thermal	82 H	1000 001x b
+3VS	GPU External Thermal	9A H	1001 101x b
+3VS	GPU External Thermal	9A H	1001 101x b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW





LOTES_ACA-ZIF-109-P12-A_FS1R2

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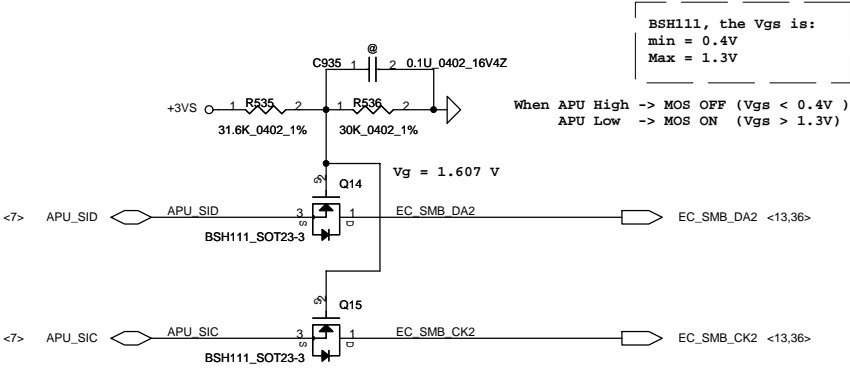
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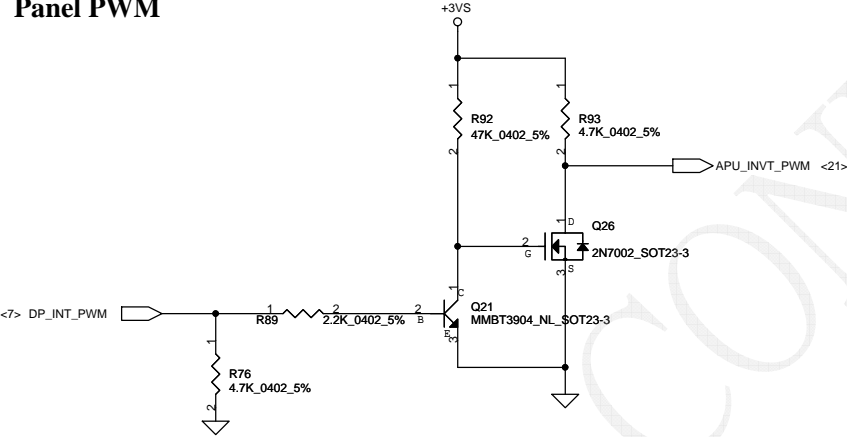
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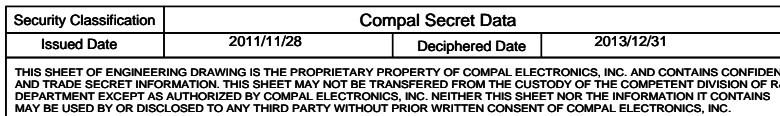
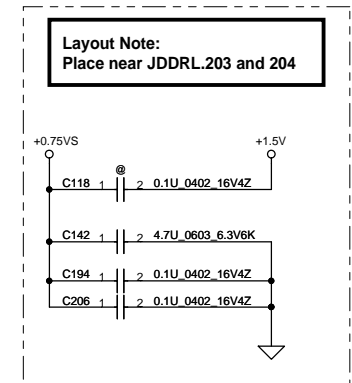
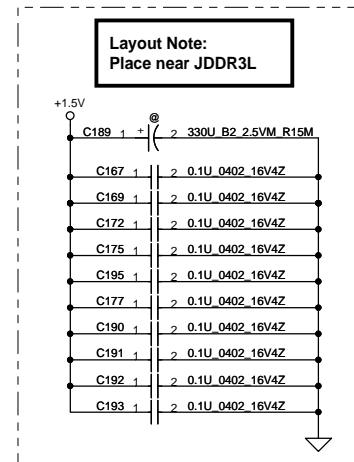
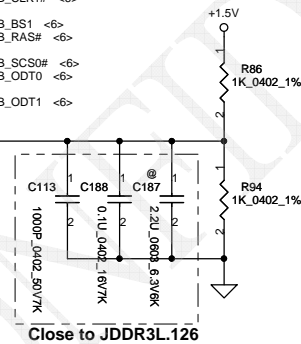
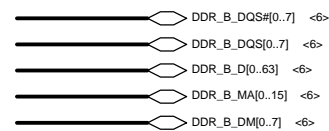
CPU TSI interface level shift



Panel PWM



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Title			
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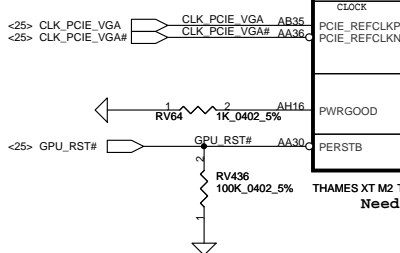
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PCIE GTX_C_CRX_P[0..15] PCIE GTX_C_CRX_P[0..15] <5>
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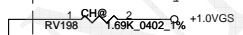
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PCIE GTX_C_CRX_P0 AA38	PCIE_RX0P	PCIE_TX0P	Y33 PCIE GTX_C_CRX_P0 0.1U 0402 16V7K 2	1 CV73	PCIE GTX_C_CRX_P0
PCIE GTX_C_CRX_N0 Y37	PCIE_RX0N	PCIE_TX0N	Y32 PCIE GTX_C_CRX_N0 0.1U 0402 16V7K 2	1 CV74	PCIE GTX_C_CRX_N0
PCIE GTX_C_CRX_P1 Y35	PCIE_RX1P	PCIE_TX1P	W33 PCIE GTX_C_CRX_P1 0.1U 0402 16V7K 2	1 CV71	PCIE GTX_C_CRX_P1
PCIE GTX_C_CRX_N1 W36	PCIE_RX1N	PCIE_TX1N	W32 PCIE GTX_C_CRX_N1 0.1U 0402 16V7K 2	1 CV72	PCIE GTX_C_CRX_N1
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PCIE GTX_C_CRX_N2 V37	PCIE_RX2N	PCIE_TX2N	U32 PCIE GTX_C_CRX_N2 0.1U 0402 16V7K 2	1 CV70	PCIE GTX_C_CRX_N2
PCIE GTX_C_CRX_P3 V35	PCIE_RX3P	PCIE_TX3P	U30 PCIE GTX_C_CRX_P3 0.1U 0402 16V7K 2	1 CV67	PCIE GTX_C_CRX_P3
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PCIE GTX_C_CRX_P5 T35	PCIE_RX5P	PCIE_TX5P	T30 PCIE GTX_C_CRX_P5 0.1U 0402 16V7K 2	1 CV63	PCIE GTX_C_CRX_P5
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PCIE GTX_C_CRX_N6 P37	PCIE_RX6N	PCIE_TX6N	P32 PCIE GTX_C_CRX_N6 0.1U 0402 16V7K 2	1 CV62	PCIE GTX_C_CRX_N6
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PCIE GTX_C_CRX_N7 N36	PCIE_RX7N	PCIE_TX7N	P29 PCIE GTX_C_CRX_N7 0.1U 0402 16V7K 2	1 CV60	PCIE GTX_C_CRX_N7
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PCIE GTX_C_CRX_N9 L36	PCIE_RX9N	PCIE_TX9N	N29 PCIE GTX_C_CRX_N9 0.1U 0402 16V7K 2	1 CV56	PCIE GTX_C_CRX_N9
PCIE GTX_C_CRX_P10 L38	PCIE_RX10P	PCIE_TX10P	L33 PCIE GTX_C_CRX_P10 0.1U 0402 16V7K 2	1 CV53	PCIE GTX_C_CRX_P10
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PCIE GTX_C_CRX_P11 K35	PCIE_RX11P	PCIE_TX11P	L30 PCIE GTX_C_CRX_P11 0.1U 0402 16V7K 2	1 CV51	PCIE GTX_C_CRX_P11
PCIE GTX_C_CRX_N11 J36	PCIE_RX11N	PCIE_TX11N	L29 PCIE GTX_C_CRX_N11 0.1U 0402 16V7K 2	1 CV52	PCIE GTX_C_CRX_N11
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PCI EXPRESS INTERFACE



Chelsea Only

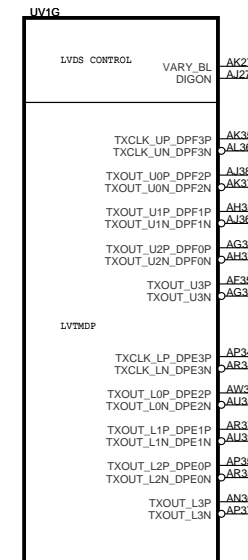


Thames Only

Install 2K for Thames/Seymour

RV65
1K 0402 1%
CH@

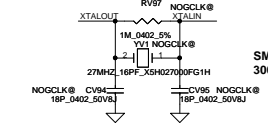
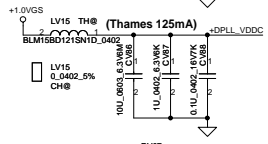
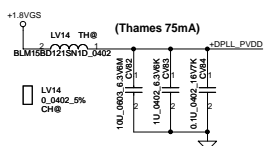
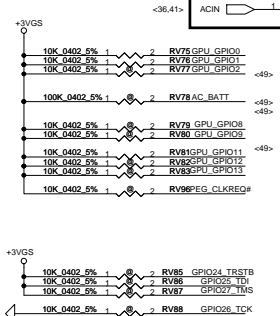
LVDS Interface



THAMES XT M2 TH@

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STRAPS



SM010009U00
300mA 120ohm@100mhz DCR 0.3

R802 place near YV1

UV18

M71 GFX

I2C

SCL

SDA

GENERAL PURPOSE I/O

GPIO_0

GPIO_1

GPIO_2

GPIO_3 SMBDATA

GPIO_4 SMBCLK

GPIO_5 AC_BATT

GPIO_6

GPIO_7 BLON

GPIO_8 ROMSO

GPIO_9 ROMSI

GPIO_10 ROMSCK

GPIO_11

GPIO_12

GPIO_13

GPIO_14 HP02

GPIO_15 PWRONTL_0

GPIO_16

GPIO_17 THERMALNT_0

GPIO_18 HP03

GPIO_19 CTF

GPIO_20 PWRONTL_1

GPIO_21 BB_EN

GPIO_22 ROMCSB

GPIO_23 CLKREQB

GPIO_24 TRSTB

GPIO_25 TMS

GPIO_26 TCK

GPIO_27 TMS

GPIO_28 TDO

GPIO_29

GPIO_30

GPIO_31

GPIO_32

GPIO_33

GPIO_34

GPIO_35

GPIO_36

GPIO_37

GPIO_38

GPIO_39

GPIO_40

GPIO_41

GPIO_42

GPIO_43

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GPIO_227

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GPIO_242

GPIO_243

GPIO_244

GPIO_245

GPIO_246

GPIO_247

GPIO_248

GPIO_249

GPIO_250

GPIO_251

GPIO_252

GPIO_253

GPIO_254

GPIO_255

GPIO_256

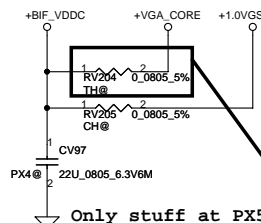
GPIO_257

<25,26,44,49> PXS_PWREN PXS_PWREN 1 RV102 0.0402_5% 2 PX_MODE PX_MODE <45,49>

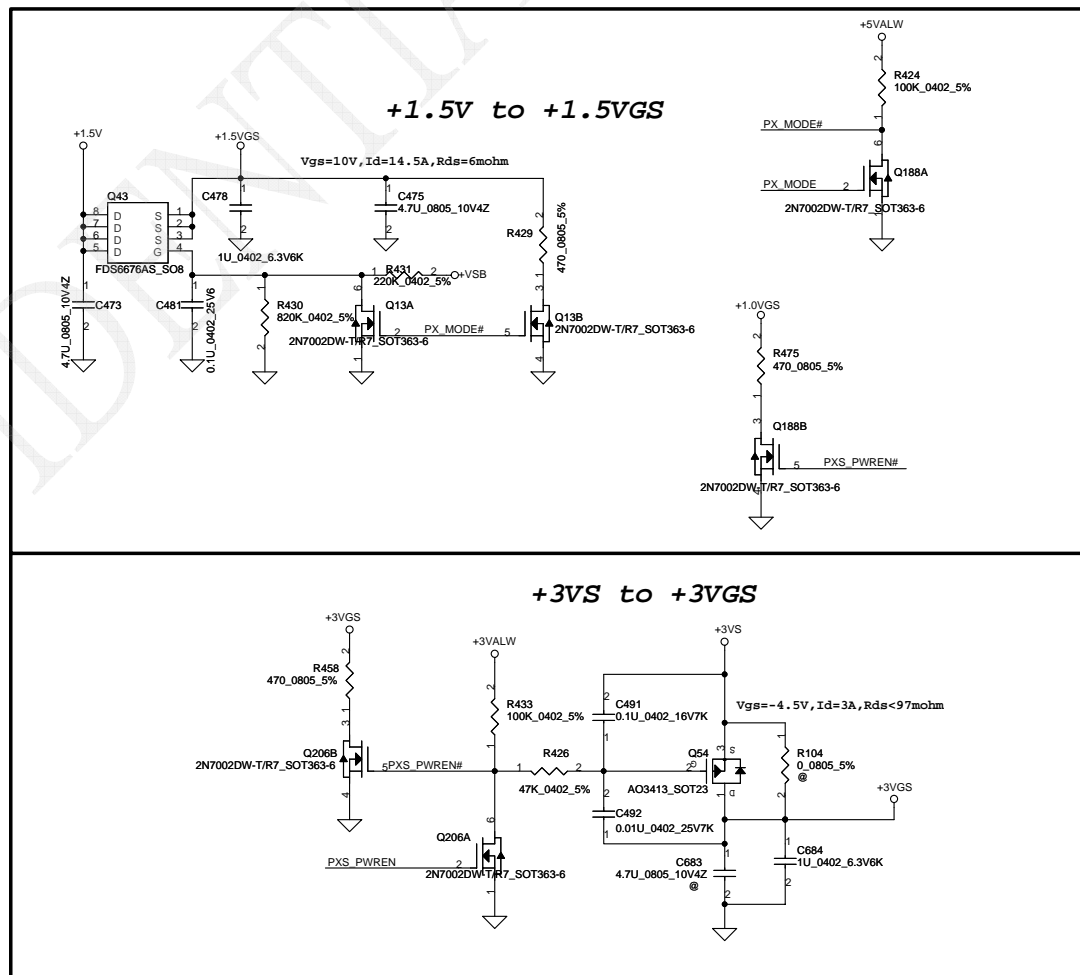
for PX5.0

PX_MODE=1 for Normal Operation

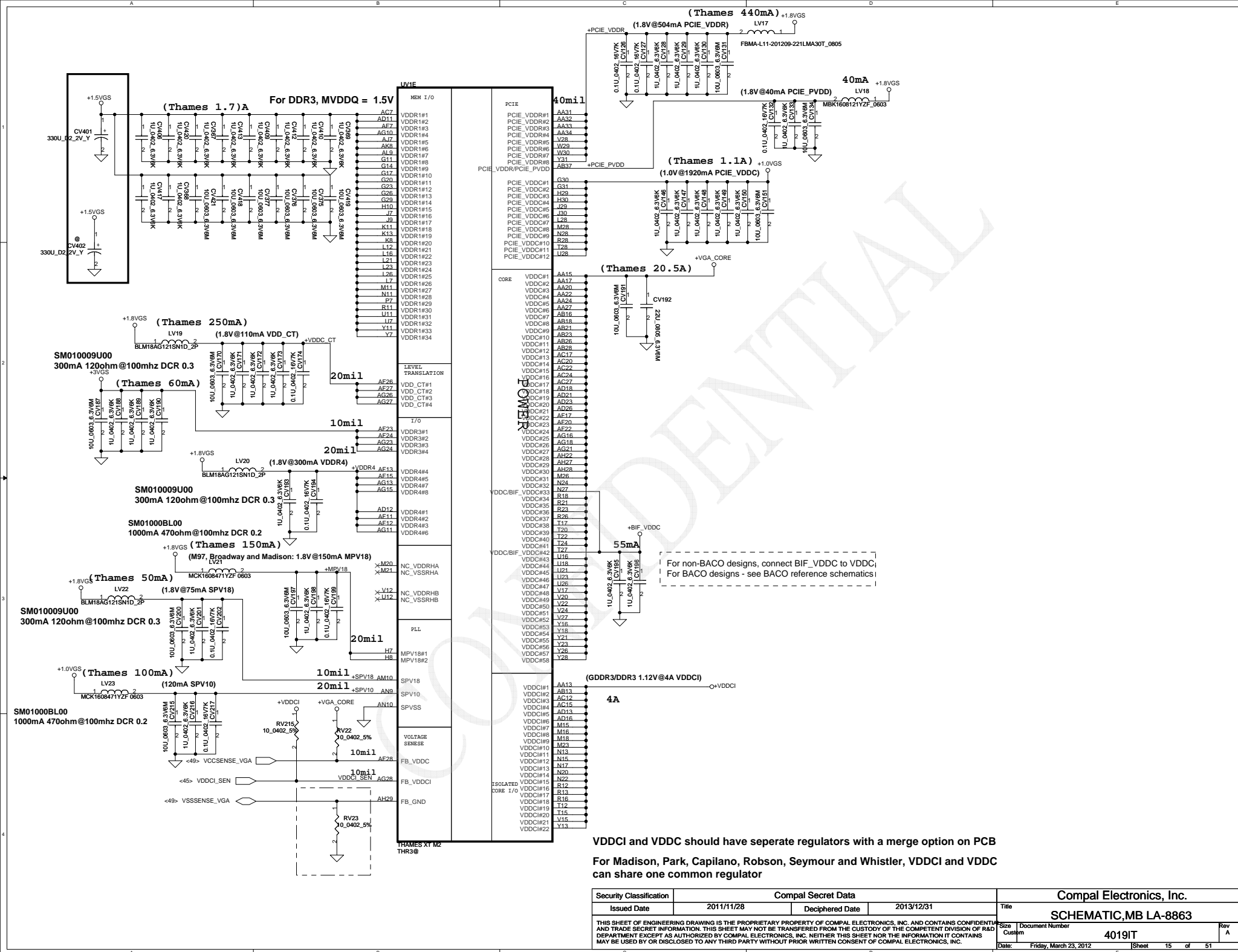
PX_MODE=0 to shut down VDDR3, PCIE_VDDC, 1.5VGS and 1.8VGS power rails

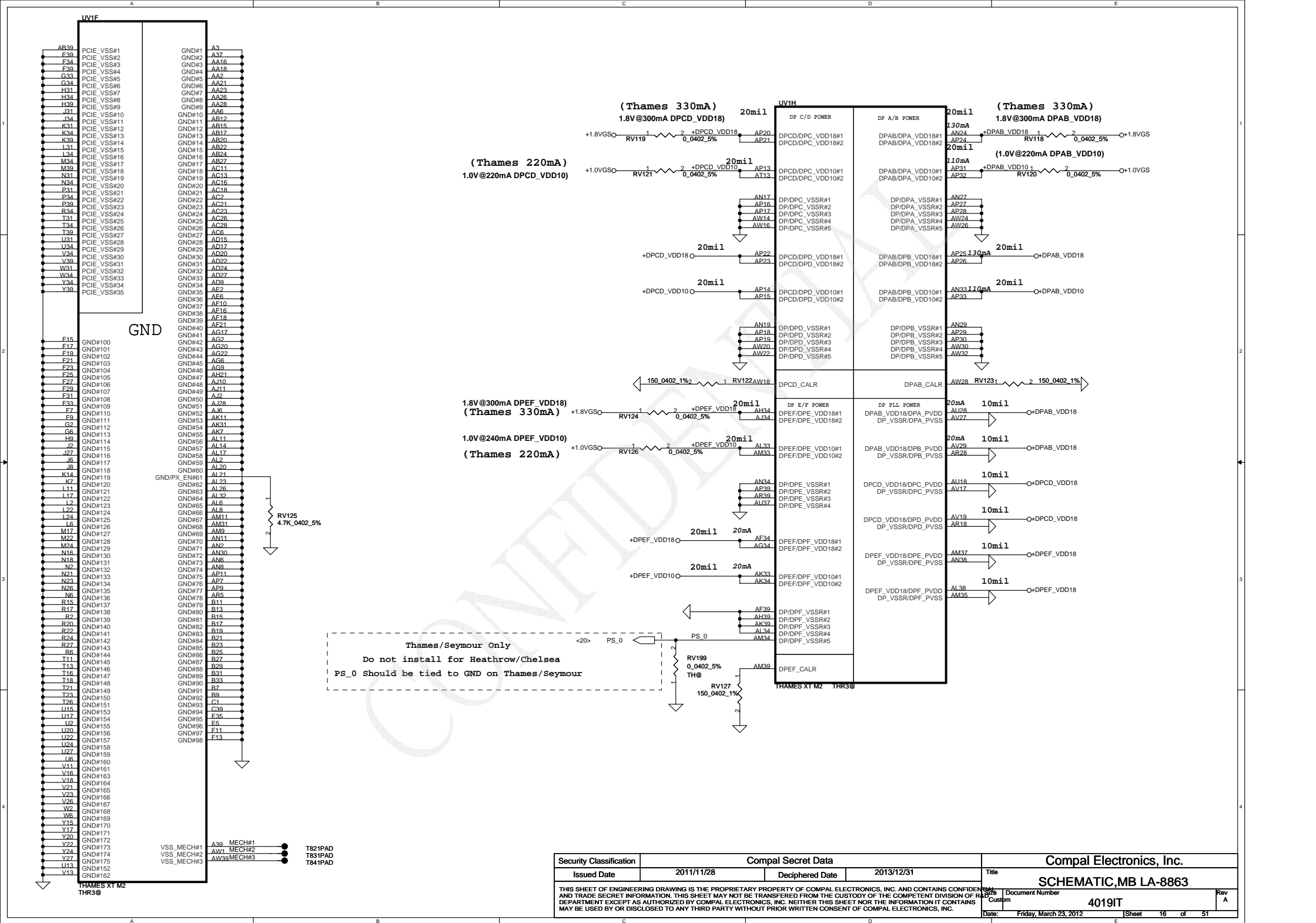


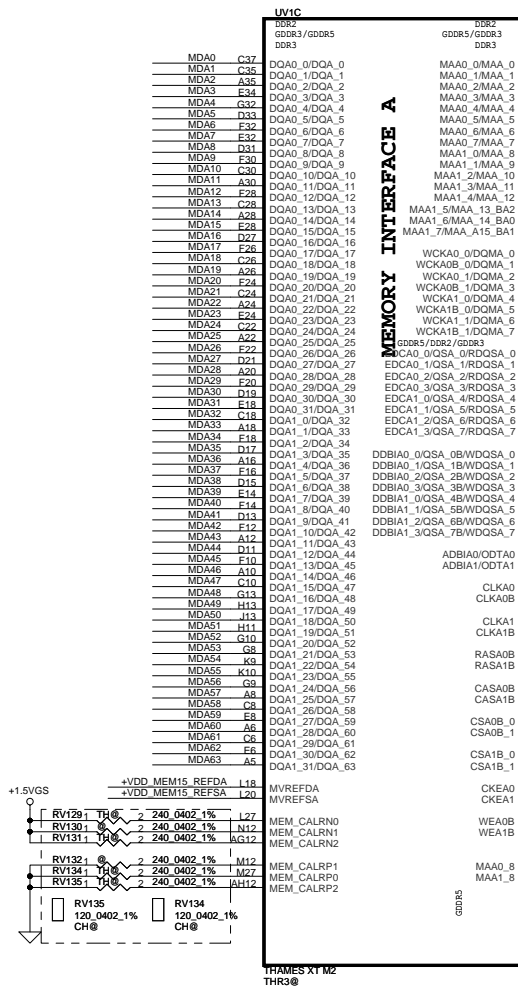
Only stuff at PX5.0 and Thames XT,
un-stuff on PX4.0



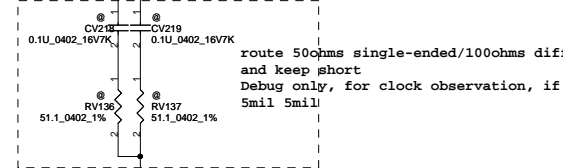
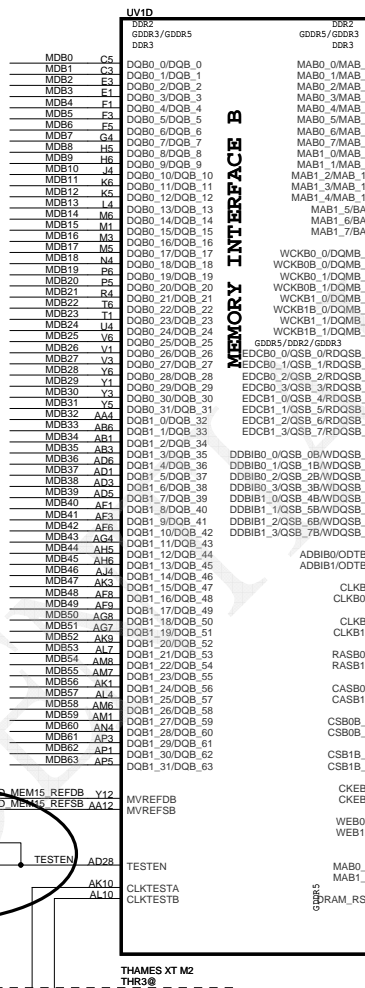
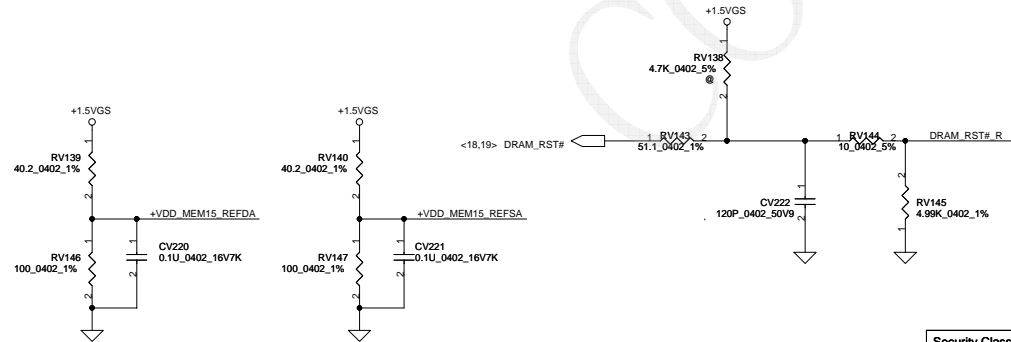
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				Date:	Friday, March 23, 2012
				Sheet	14 of 51







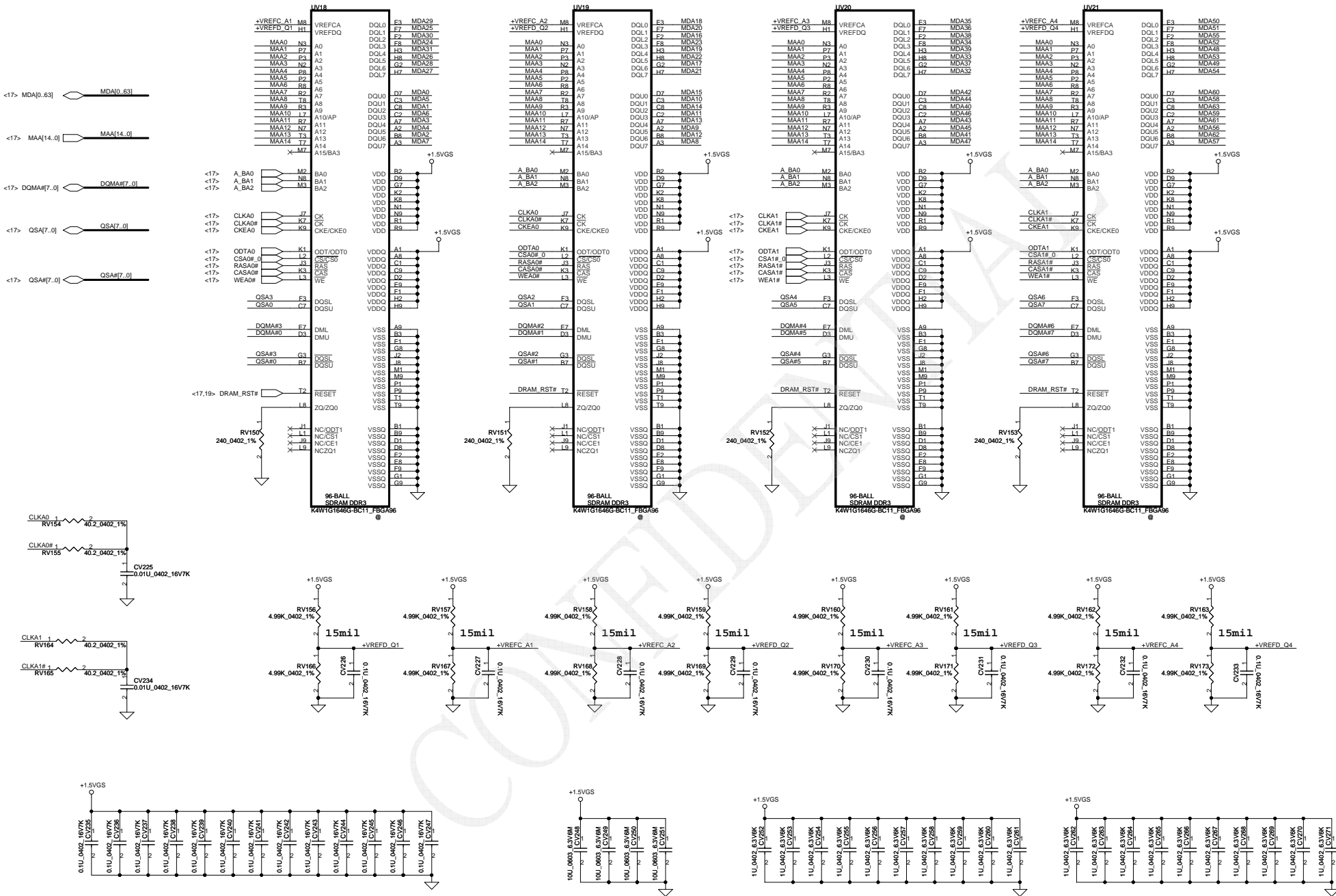
This basic topology should be used for DRAM RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and // cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



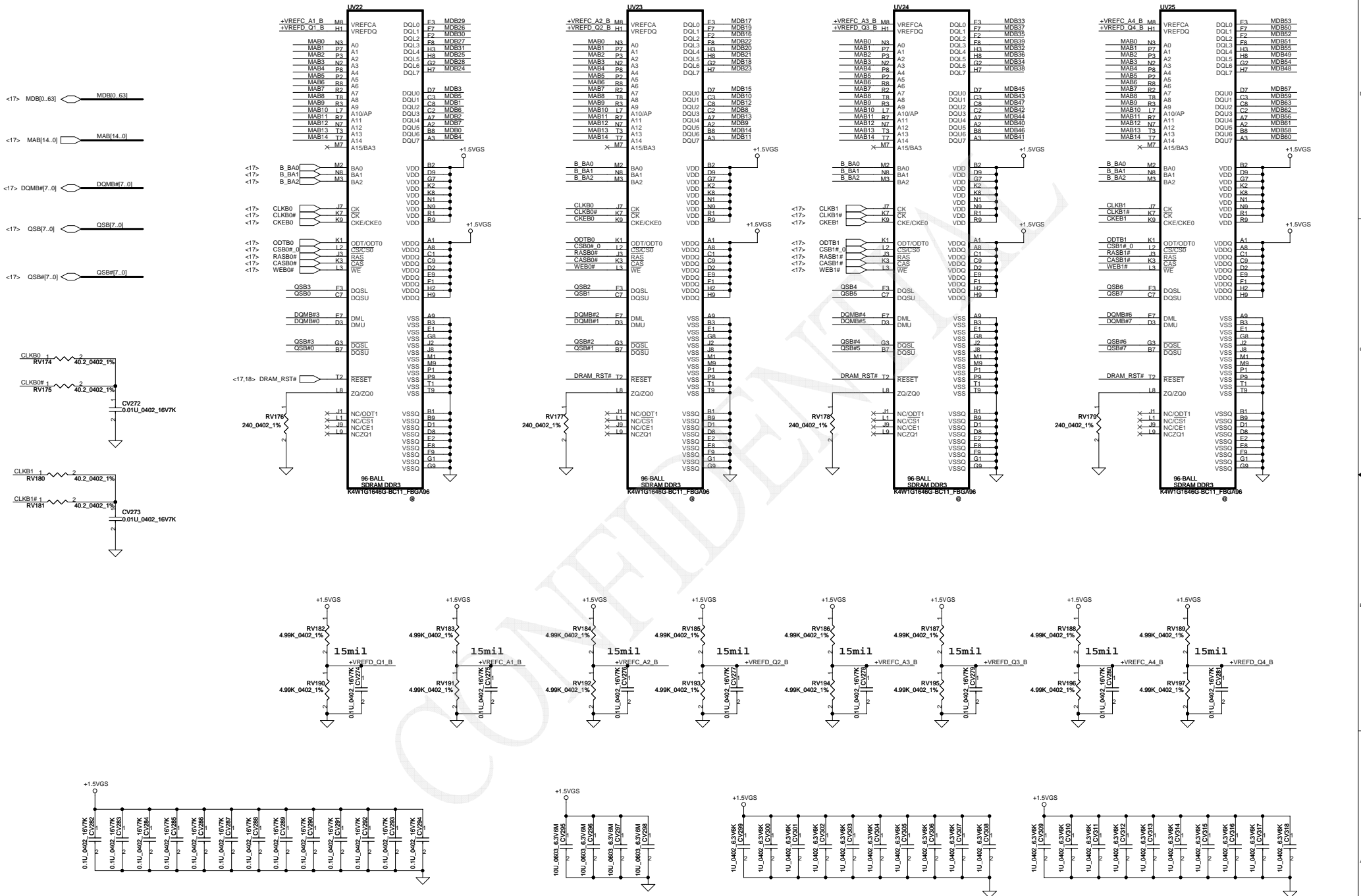
route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

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				Custom	40191T
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				Sheet	17 of 51

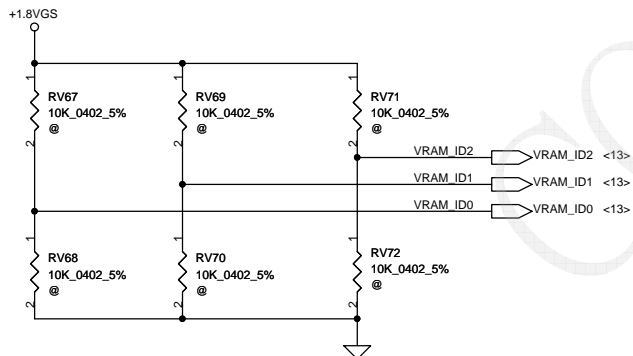
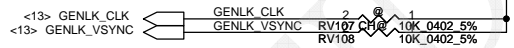
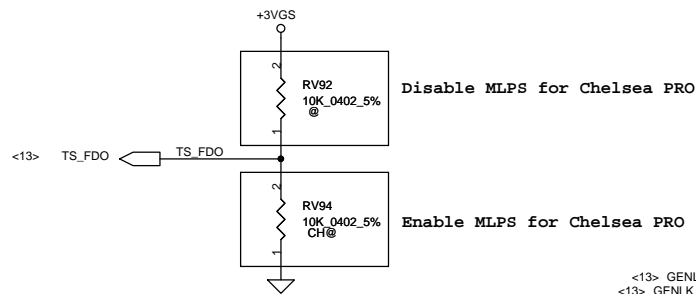
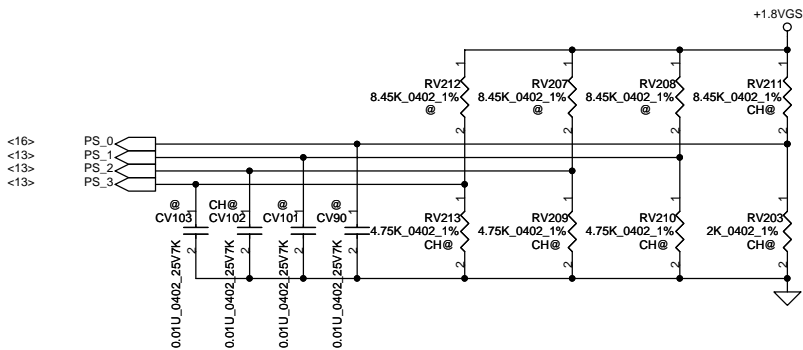
CHANNEL A: 512MB/1024MB DDR3



CHANNEL B: 512MB/1024MB DDR3



	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0	1 1	0 0 1	NC	8.45k	2k
PS_1	1 1	0 0 0	NC	NC	4.75k
PS_2	0 0	0 0 0	680 nF	NC	4.75k
PS_3	1 1	0 0 0	NC	NC	4.75k



VRAM Straps

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (1G)	H5TQ1G63DFR-11C Hynix 1GB SA000041S20	RV68 0	RV70 0	RV72 0
★64MX16 (1G)	R4W1G1646G-BC11 Samsung 1GB SA00004GS00	RV67 1	RV70 0	RV72 0
128M16 (2G)	H5TQ2G63BFR-11C Hynix 2GB SA00003YO00	RV68 0	RV69 1	RV72 0
★128M16 (2G)	R4W2G1646C-BC11 Samsung 2GB SA000047Q00	RV67 1	RV69 1	RV72 0

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

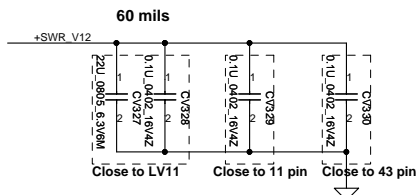
MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO2	PCIe Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO8	PCIe clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIe full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
AUD[1] AUD[0]	HSYNC VSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

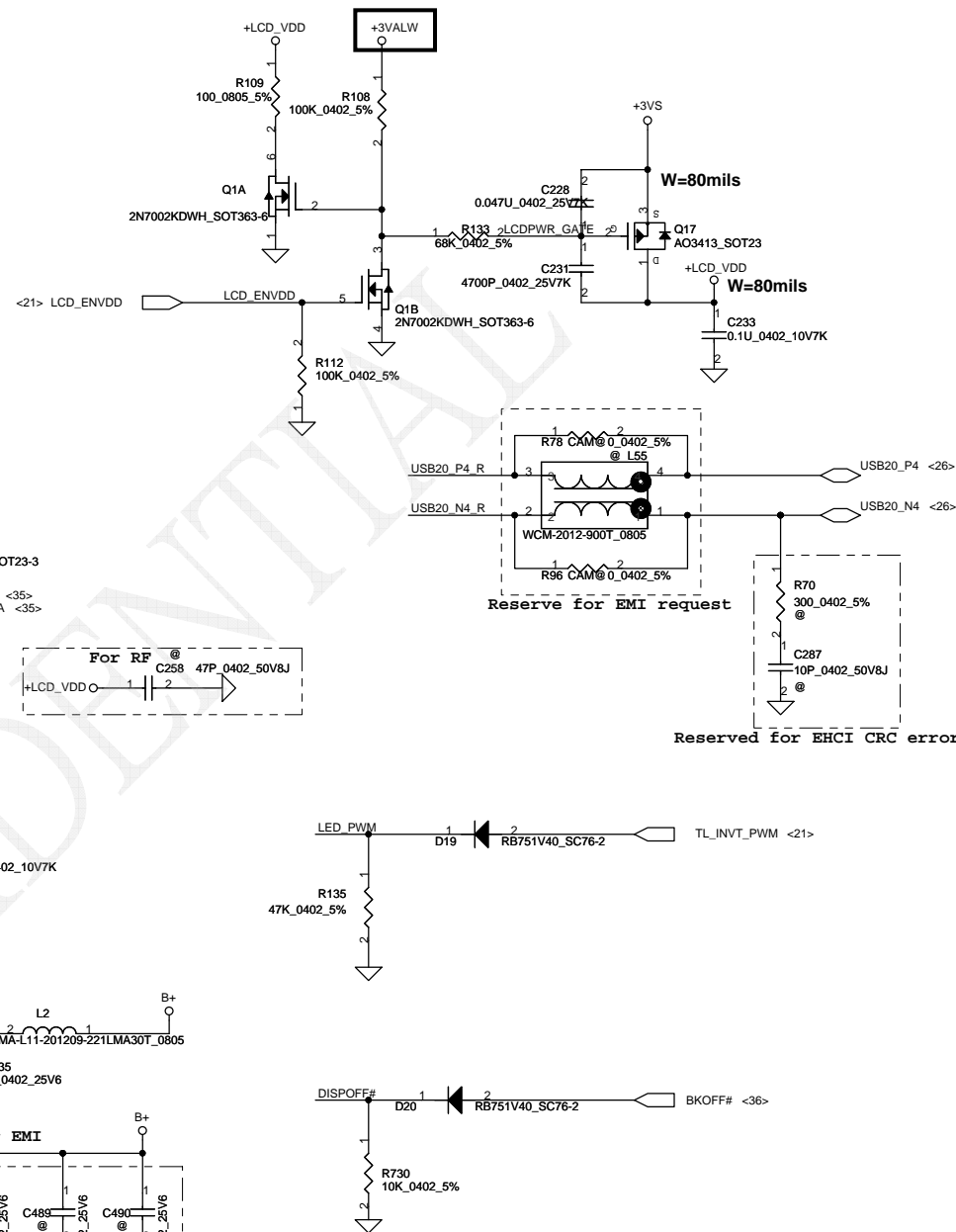
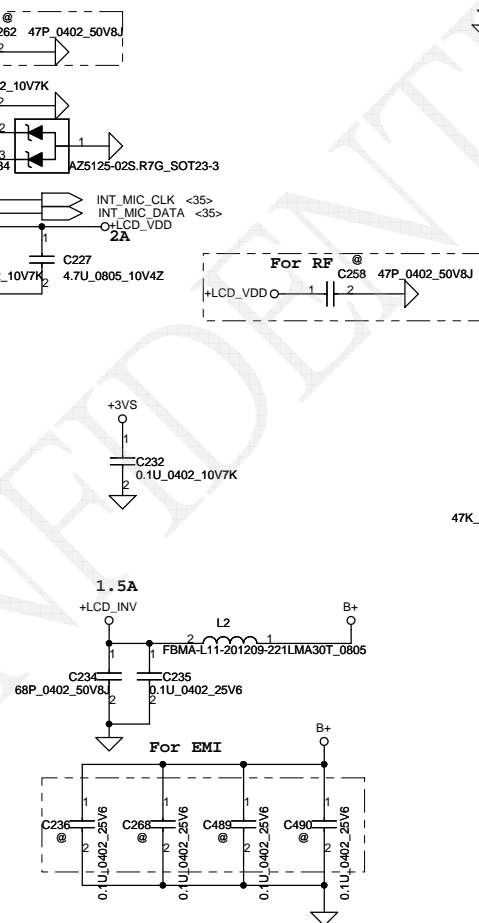
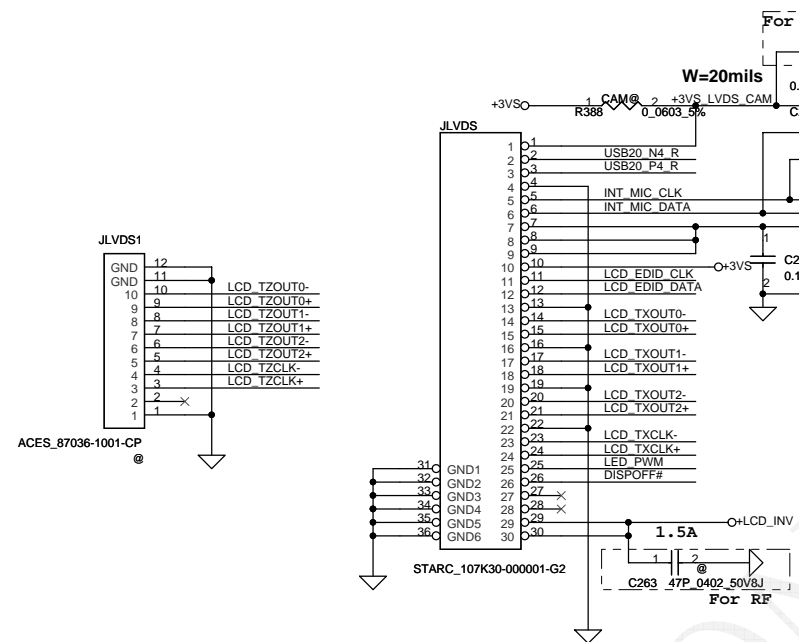
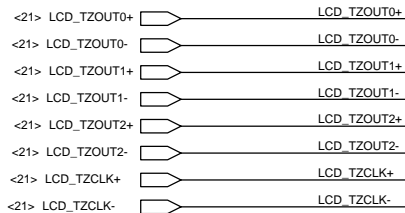
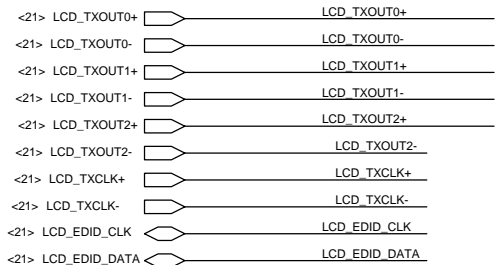
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LCD_EDID_DATA RV2811 2 4.7K 0402 5%
 LCD_EDID_CLK RV2821 2 4.7K 0402 5%
 MIIC_SDA RV2831 2 4.7K 0402 5%
 CSCL RV2851 2 4.7K 0402 5%
 CSDA RV2891 2 4.7K 0402 5%

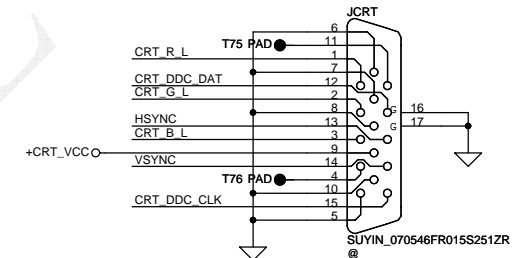
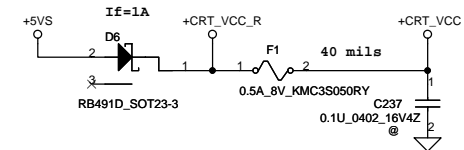


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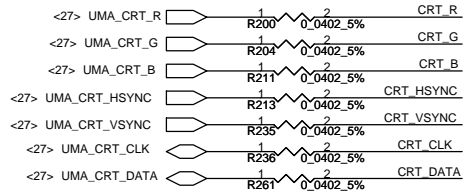


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CRT CONNECTOR

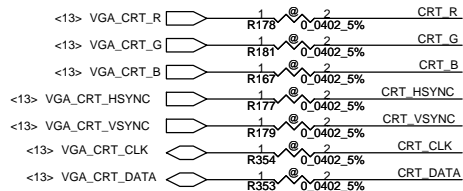


For PowerXpress

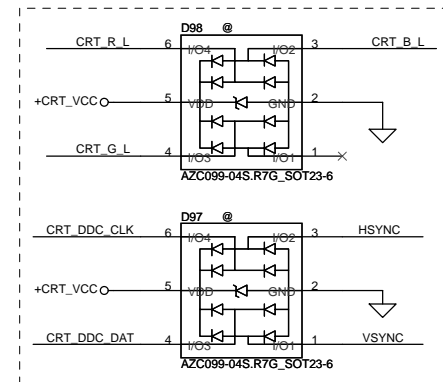
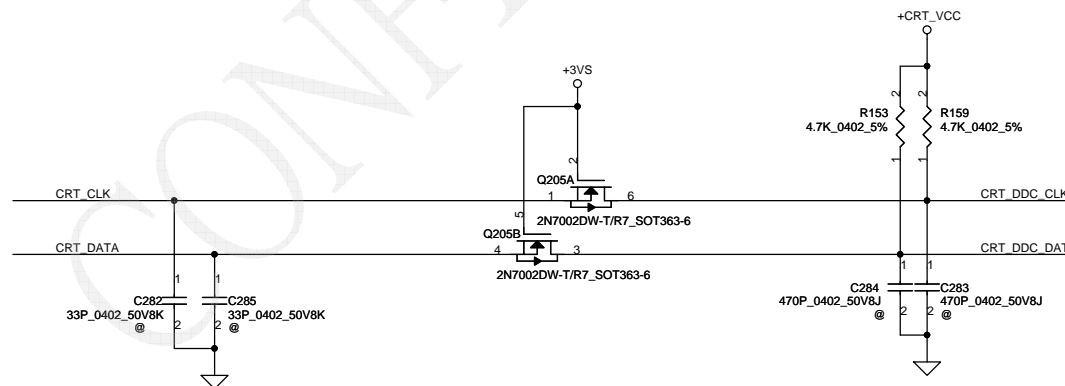
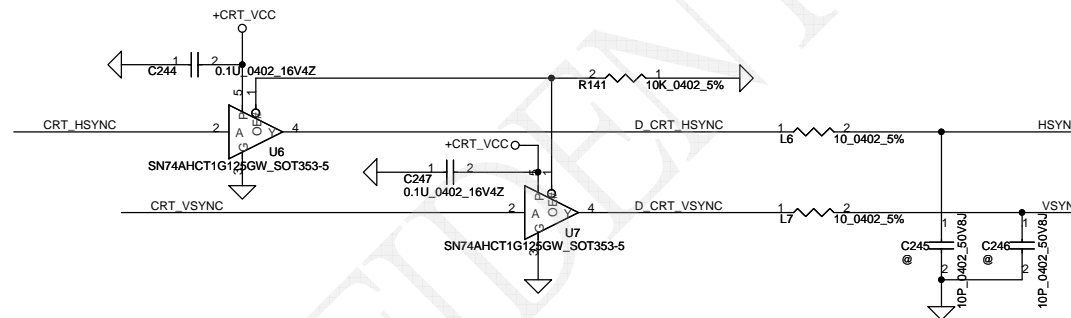
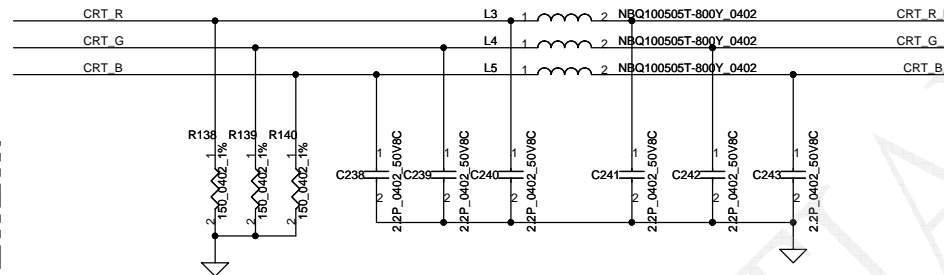


Close to CRT Connector

For Debug



Close to CRT Connector



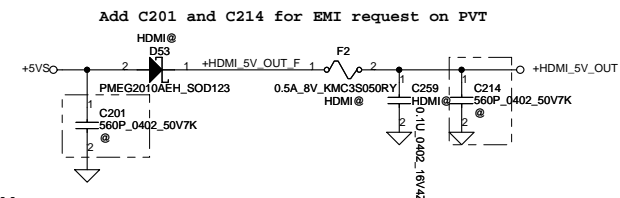
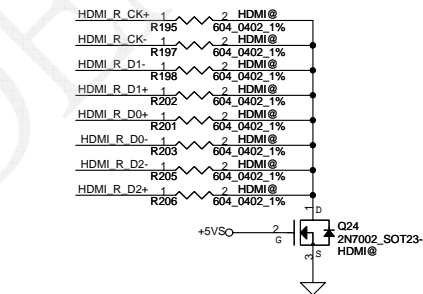
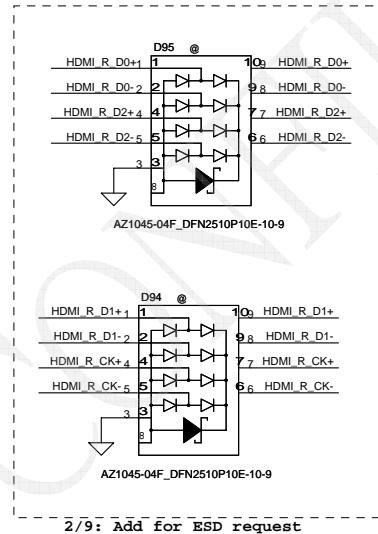
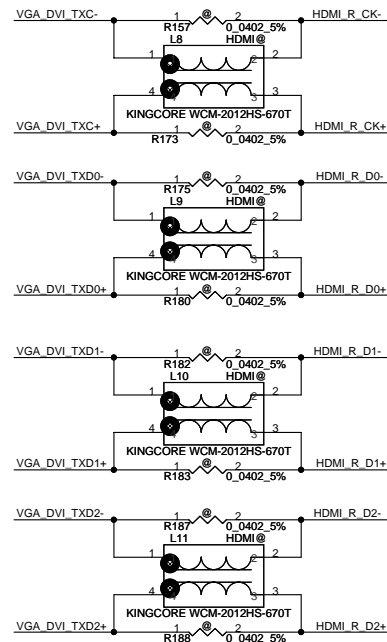
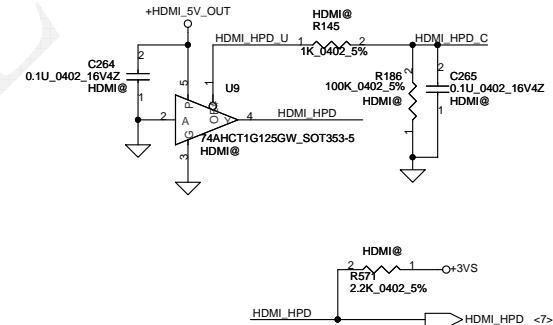
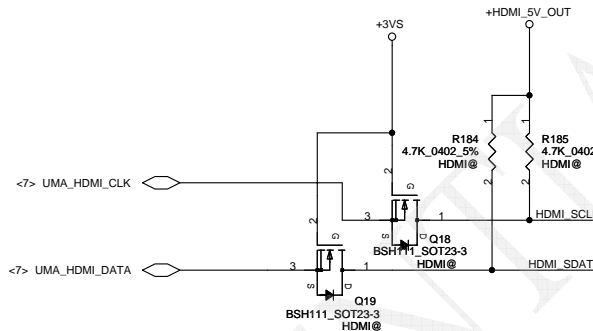
2/9: Add for ESD request

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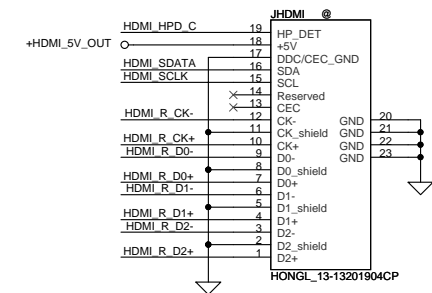
OE#	A	Y
L	L	L
L	H	H
H	X	Z

Change R184 and R185 from 2K to 4.7K
for HDMI detect issue on preMP

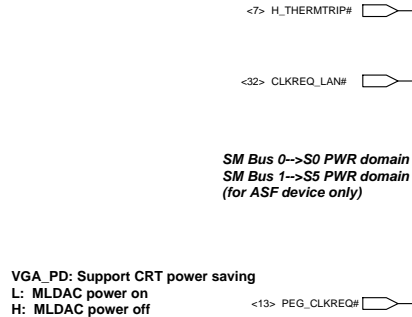
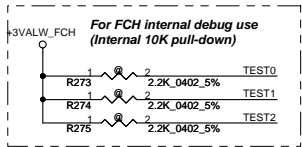
<7> UMA_HDMI_TXC+	C310	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C321	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C326	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C313	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C309	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C314	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C318	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C322	1	2	0.1U_0402_16V7K HDMI@	VGA_DVI_TXD2-



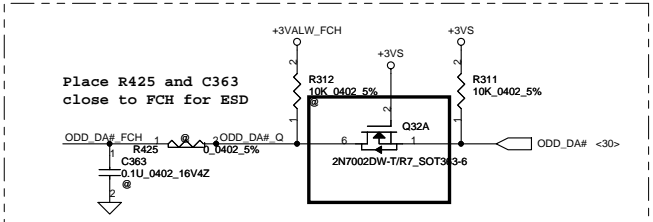
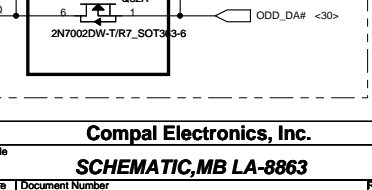
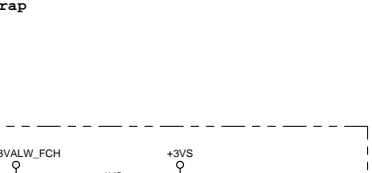
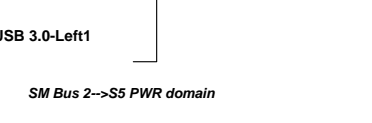
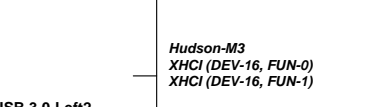
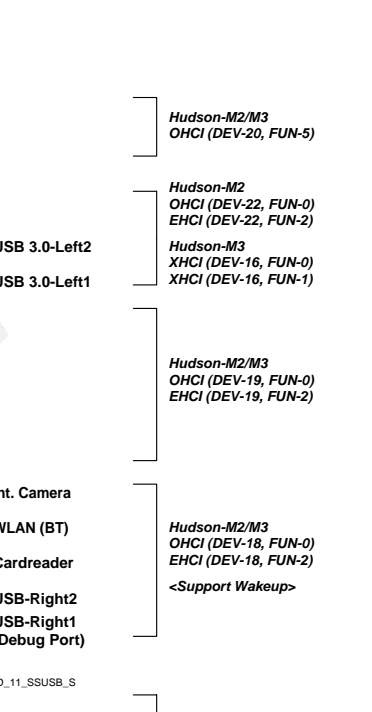
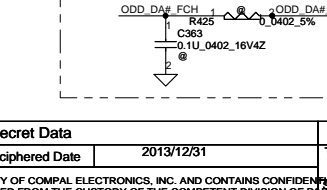
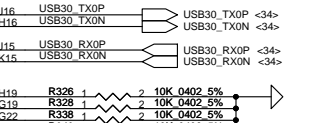
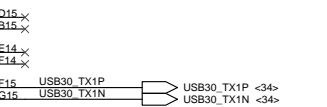
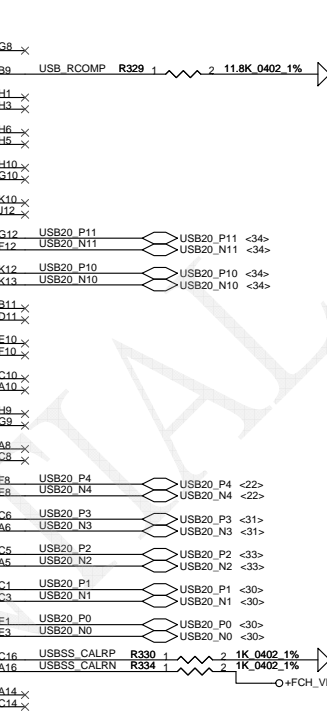
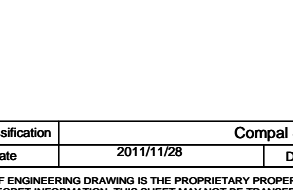
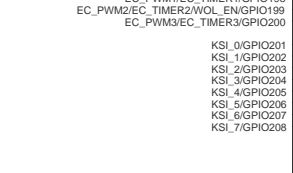
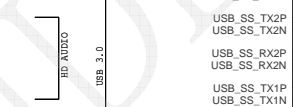
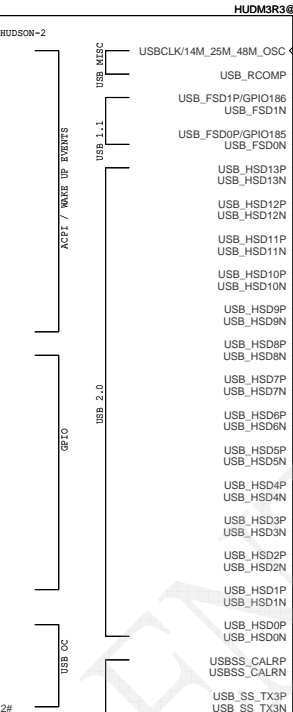
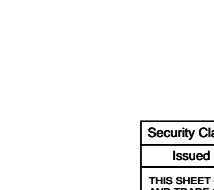
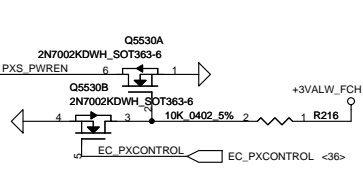
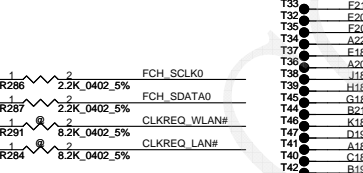
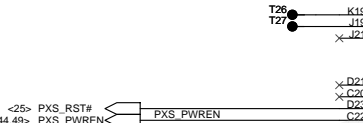
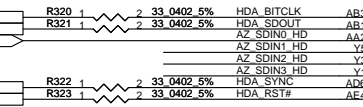
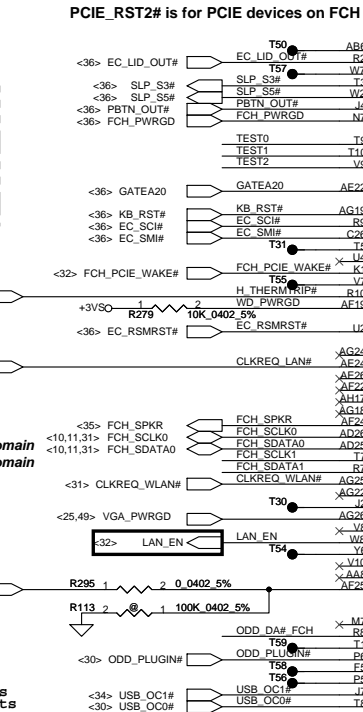
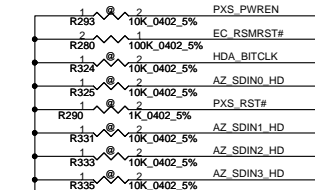
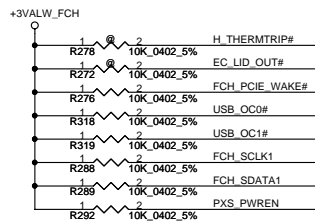
HDMI Connector



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USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports

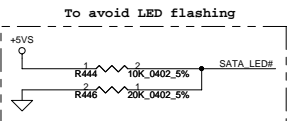
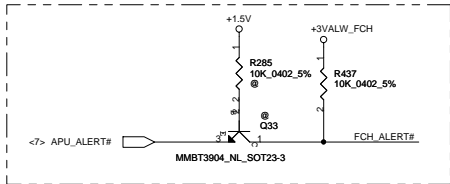


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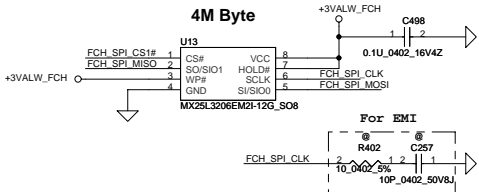
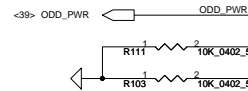
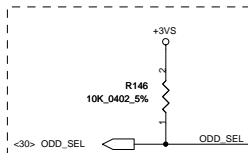
HDD

14" ODD

15"/17" ODD



ODD_SEL	SATA port	SKU
High	Port 1	14"
Low	Port 2	15"/17"



U18

HUDSON-2

ED_C3D0

GBE_COL

GBE_CRS

GBE_MDIO

GBE_RXCLK

GBE_RXD0

GBE_RXD1

GBE_RXD2

GBE_RXD3

GBE_TXD0

GBE_TXD1

GBE_TXD2

GBE_TXD3

GBE_TXD4

GBE_TXD5

GBE_TXD6

GBE_TXD7

GBE_TXD8

GBE_TXD9

GBE_TXD10

GBE_TXD11

GBE_TXD12

GBE_TXD13

GBE_TXD14

GBE_TXD15

GBE_TXD16

GBE_TXD17

GBE_TXD18

GBE_TXD19

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GBE_TXD263

GBE_TXD264

GBE_TXD265

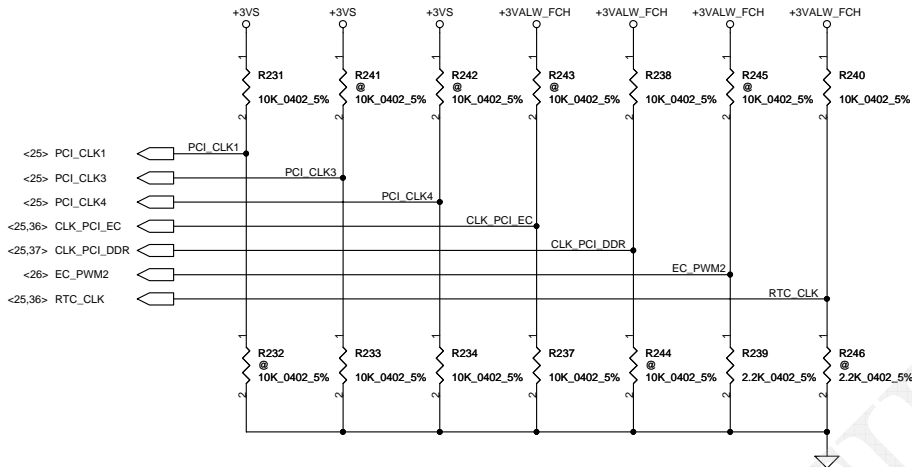
GBE_TXD266

GBE_TXD267

GBE_TXD268

STRAP PINS

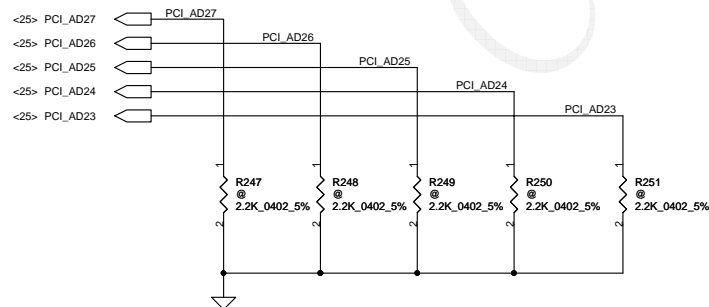
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



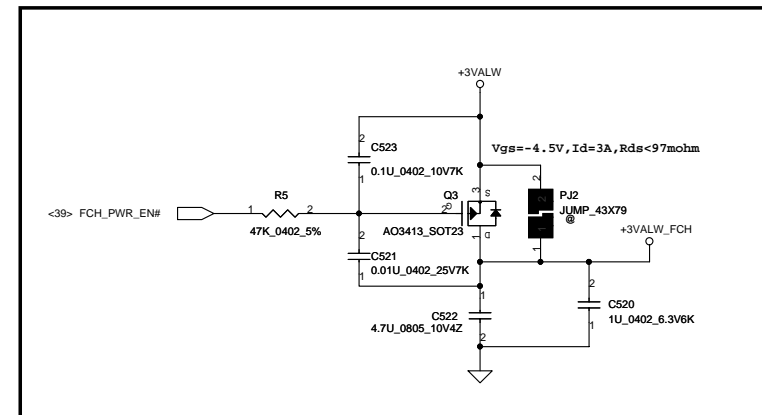
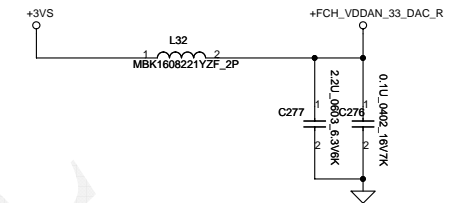
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

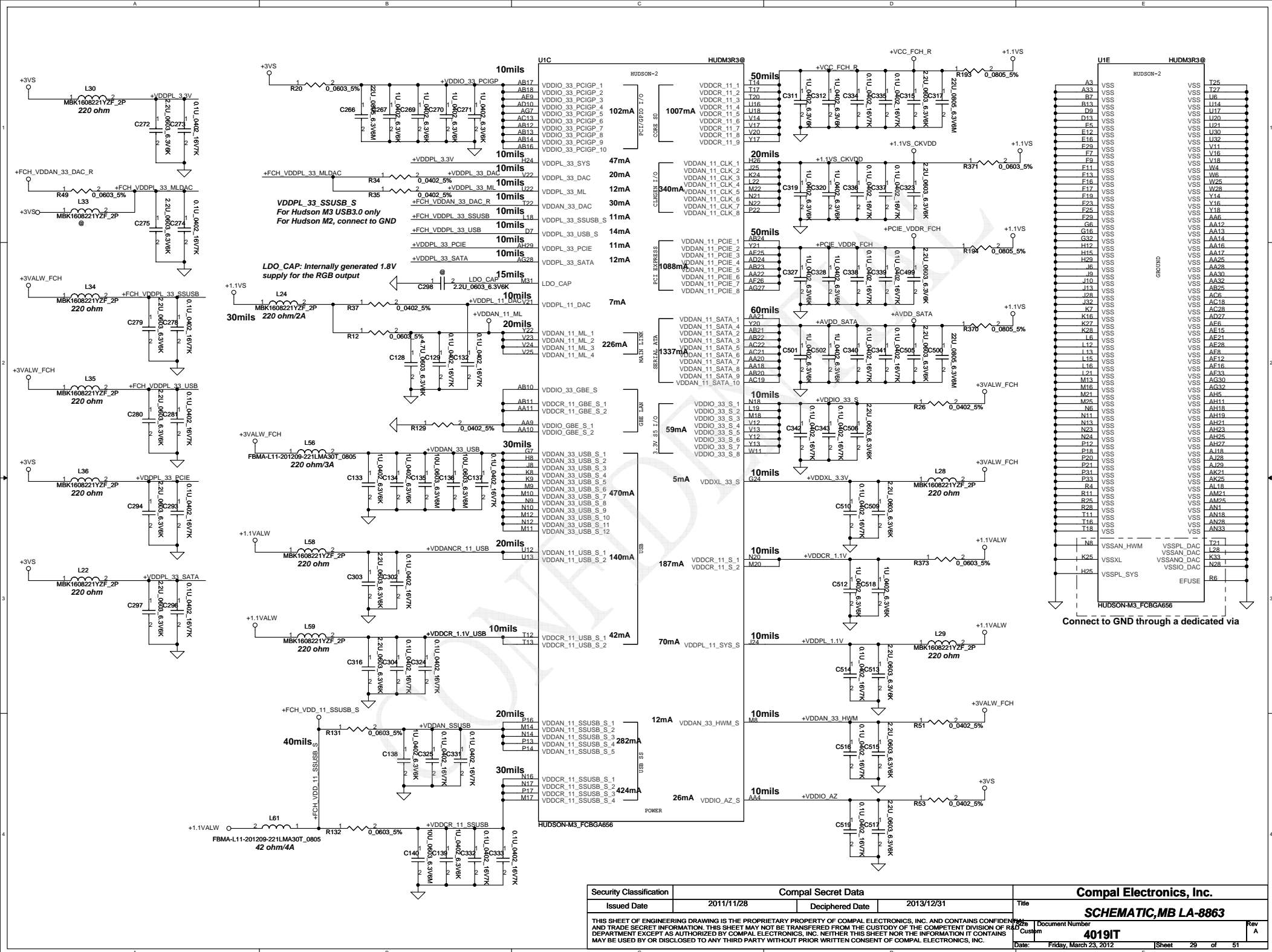
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



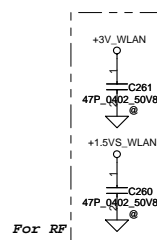
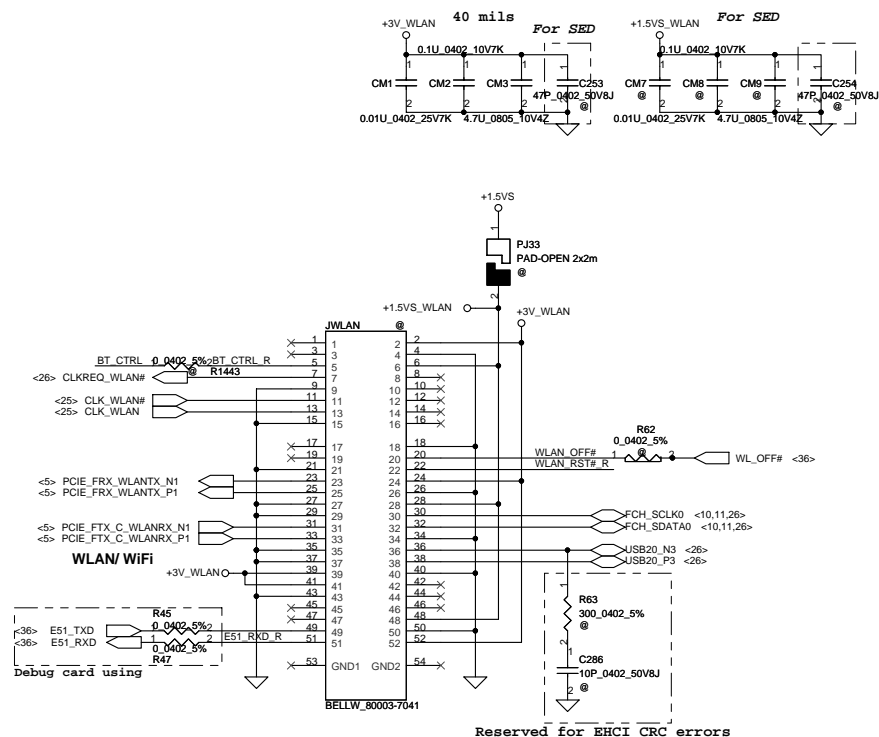
CRT Power Down Circuit




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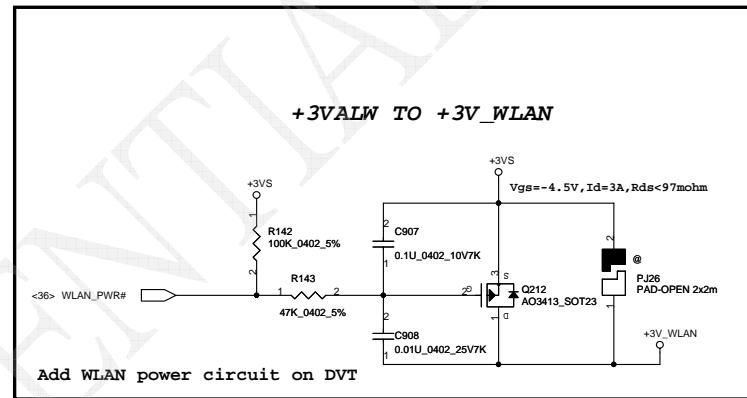
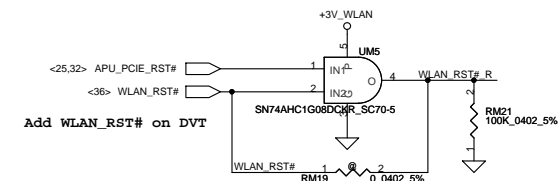
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Slot 1 Half PCIe Mini Card-WLANWLAN&BT Combo module circuits

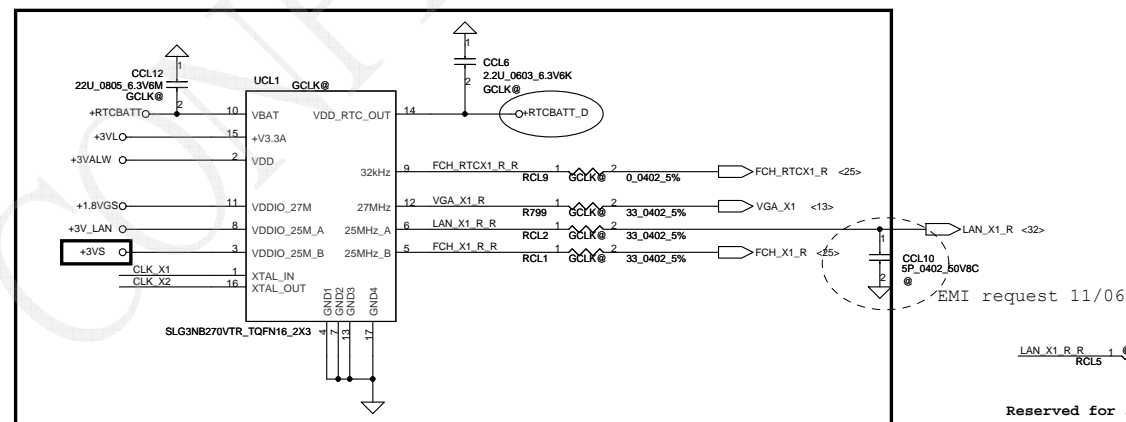
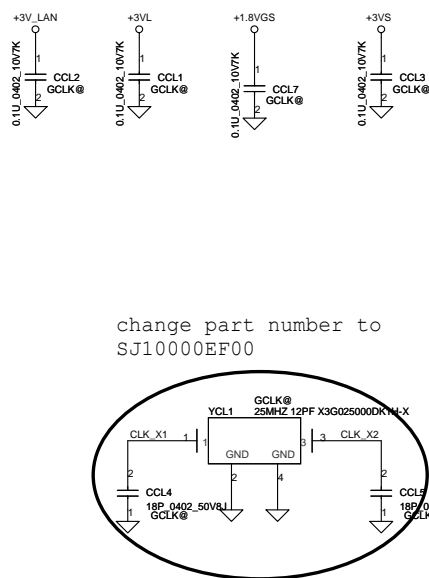
	BT on module Enable	BT on module Disable
BT_CTRL	H	L

<36> BT_CTRL  BT_CTRL 1 R337 2 E51 RXD P
1K 0402 5%

For isolate BT_CTRL and
Compal Debug Card.

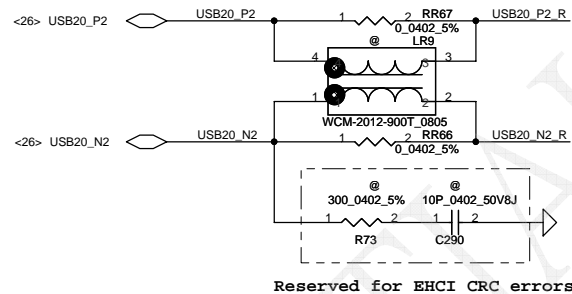
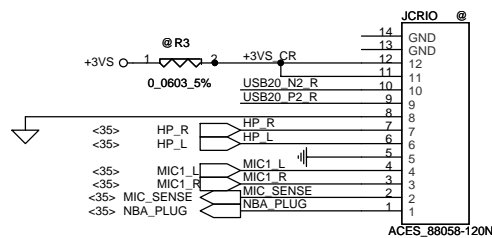


Change to GCLK to SLG3NB270V
SA00005DP00 for 27MHz
for VGA

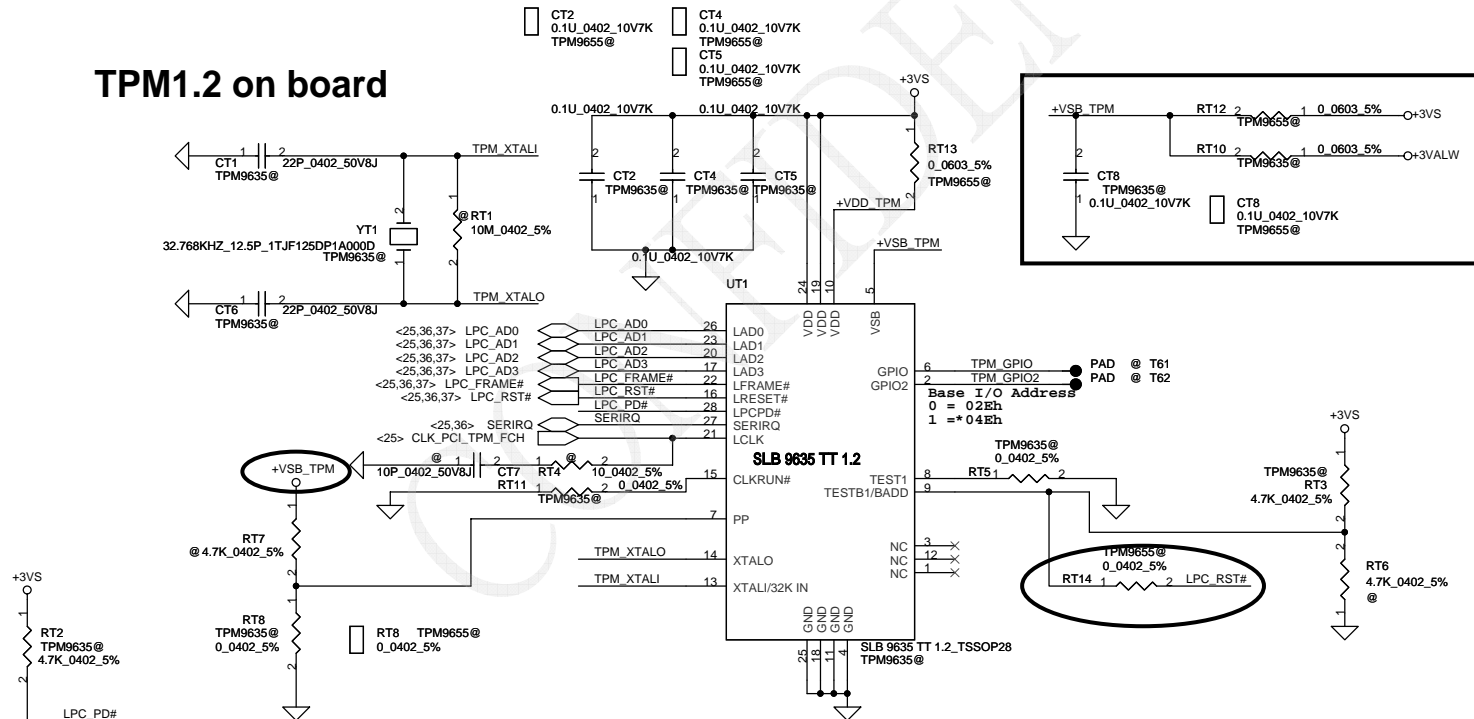


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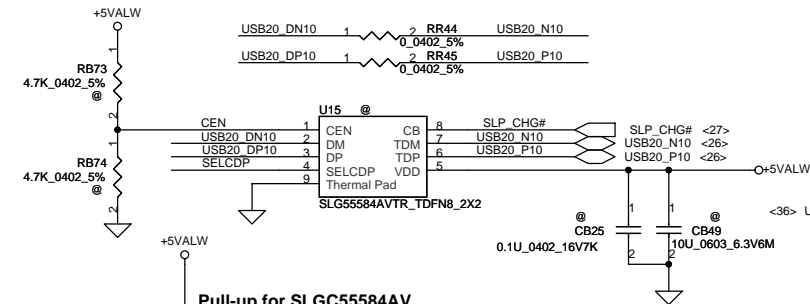
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CardReader Conn.

TPM1.2 on board



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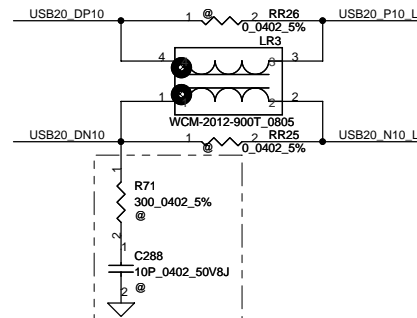
Pull-up for SLGC55584V

RB75
4.7K_0402_5%

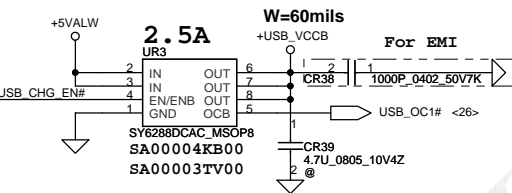
RB76
4.7K_0402_5%

Pull-down for SLGC55584V

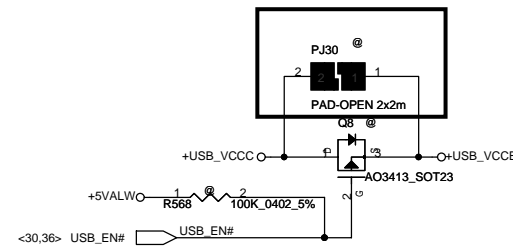
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only



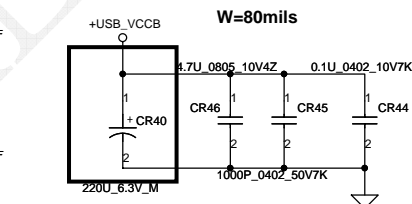
Reserved for EHCI CRC errors



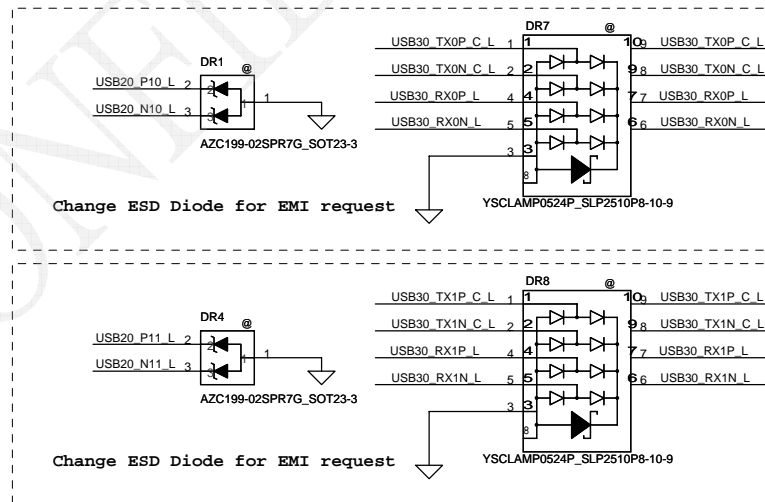
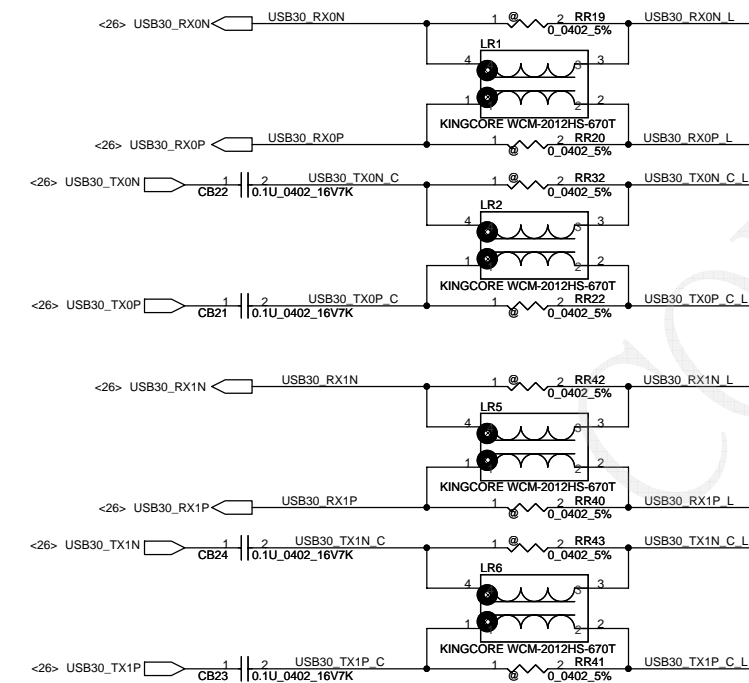
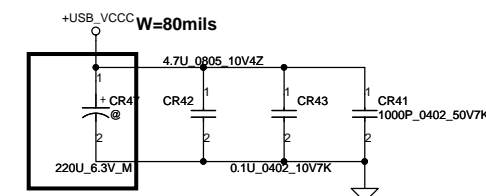
Reserved for EHCI CRC errors



W=80mils

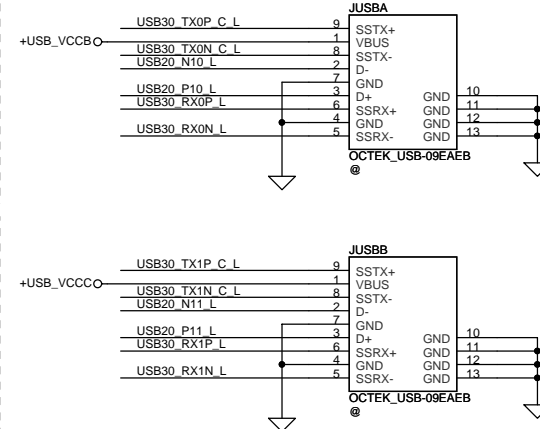


150uFx2 or 220uFx1



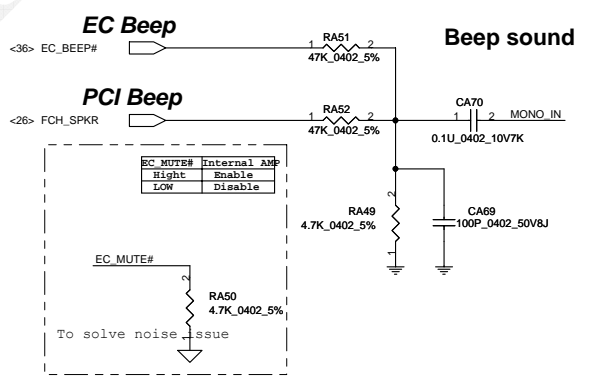
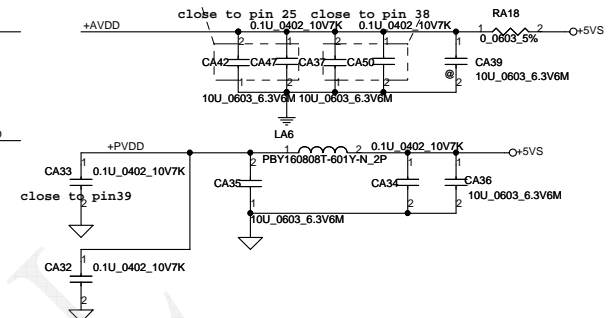
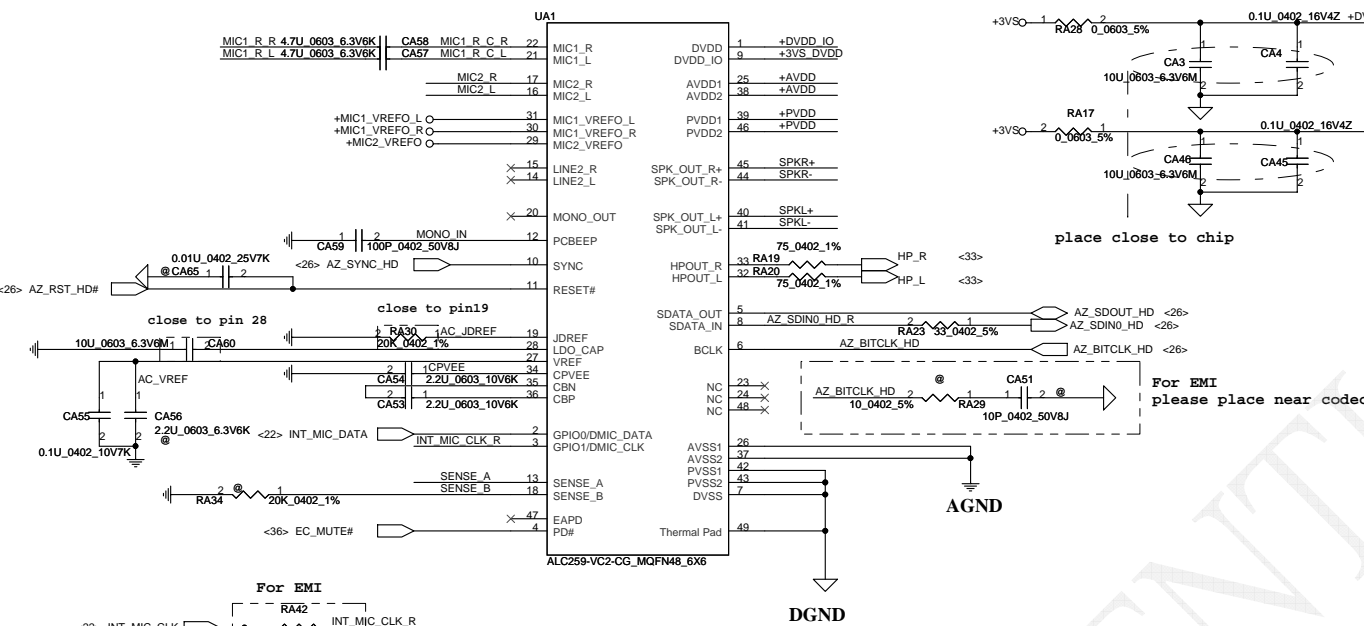
Change ESD Diode for EMI request

Change ESD Diode for EMI request

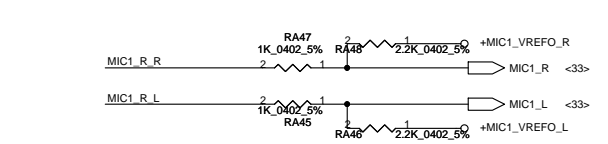


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Sheet				34				of			
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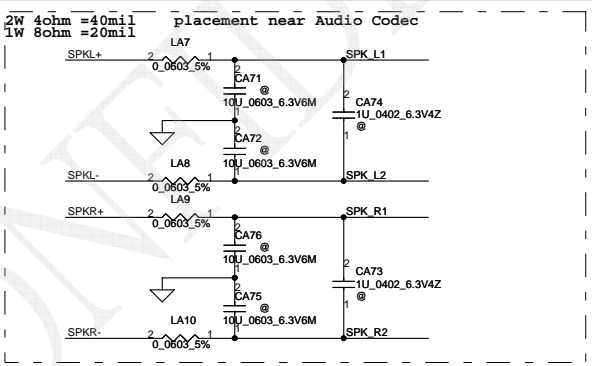
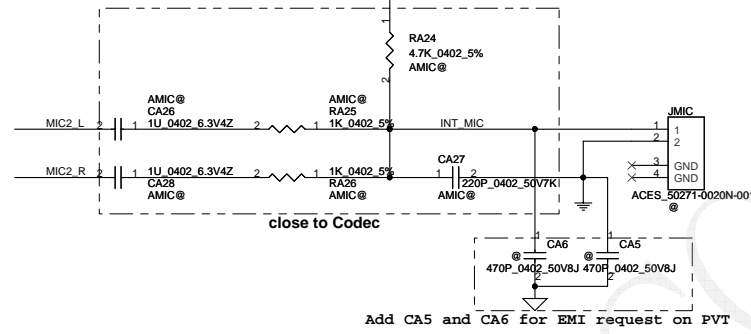
35mA for 3.3V level



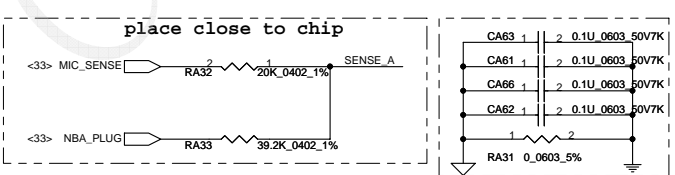
Ext.MIC/LINE IN JACK



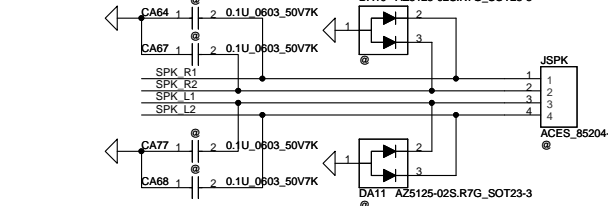
Analog MIC



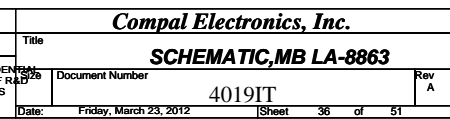
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	



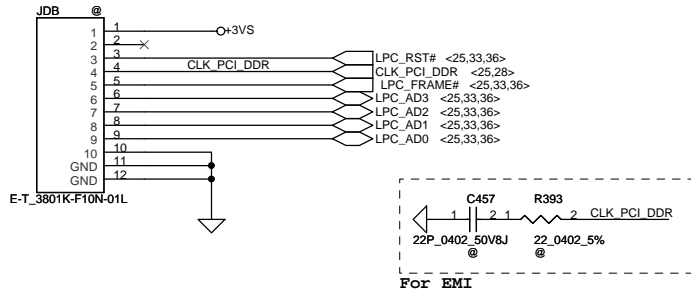
SPK Conn.



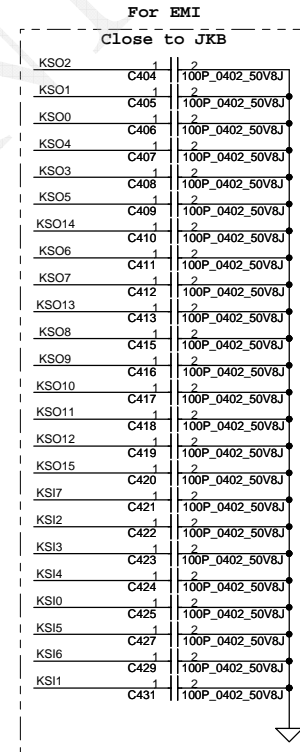
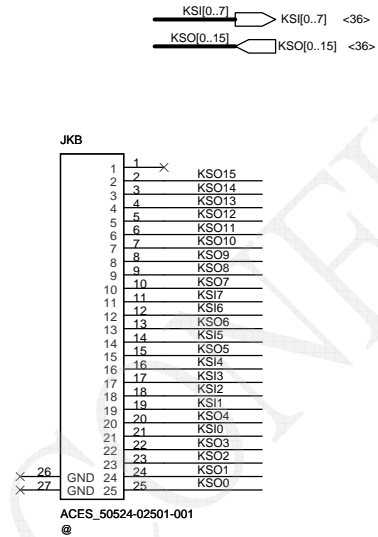
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LPC Debug Port

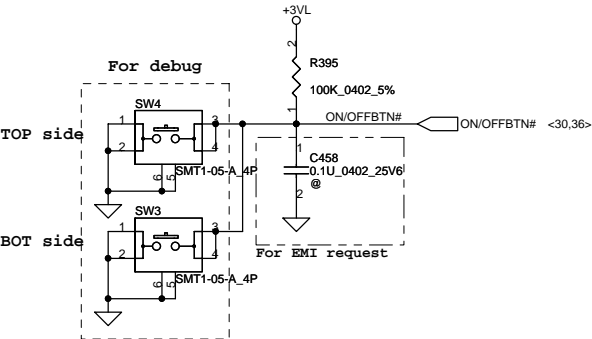


KEYBOARD CONN.

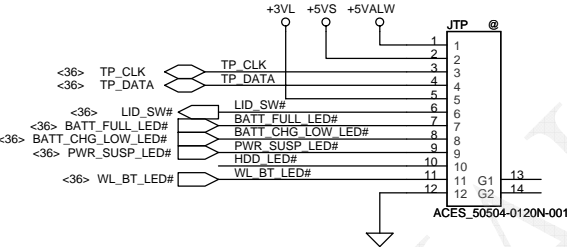


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				Size	Document Number	Rev
				A		
				Date:	Friday, March 23, 2012	Sheet 37 of 51

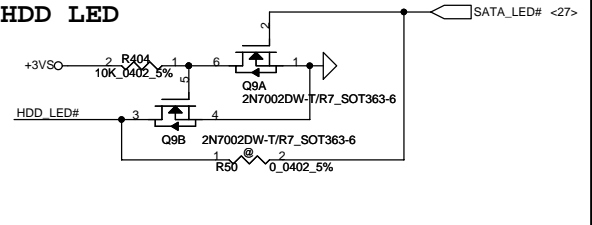
Power Button



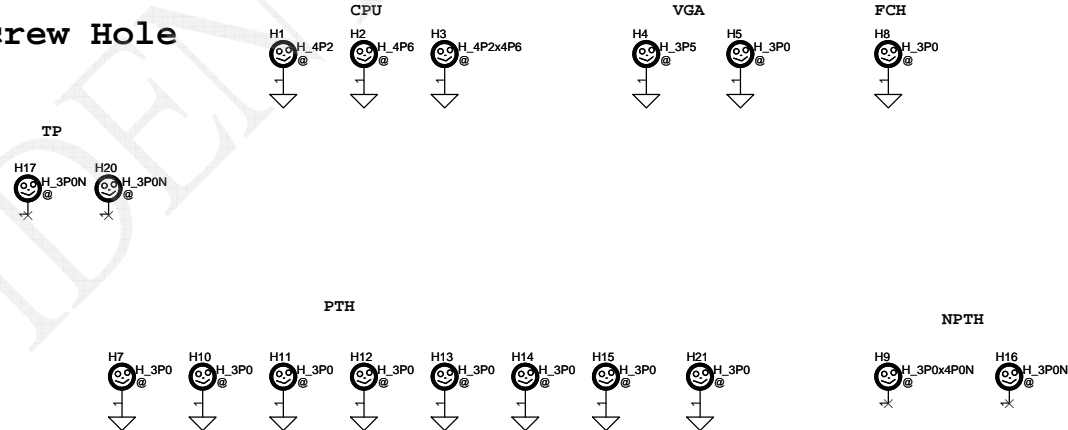
Touchpad Connector



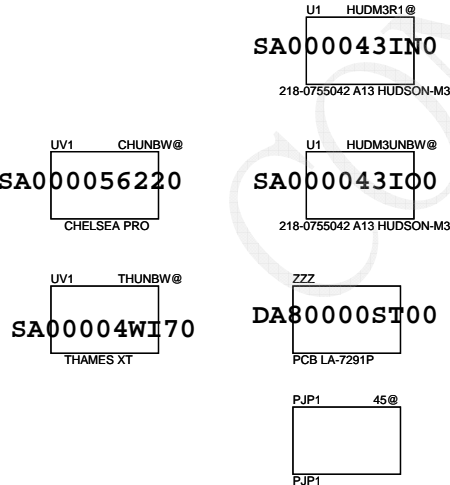
HDD LED



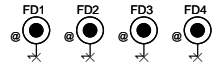
Screw Hole



ISPD

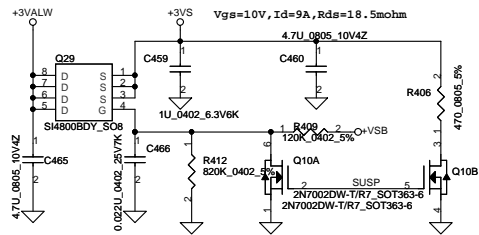


PCB Fedical Mark PAD

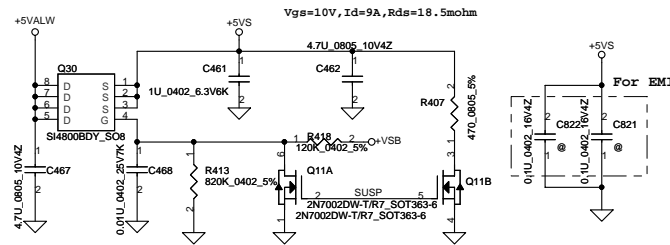


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				Date	Monday, March 26, 2012
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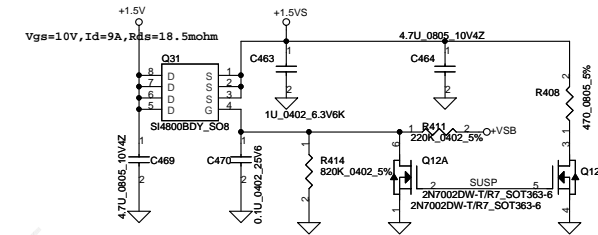
+3VALW TO +3VS



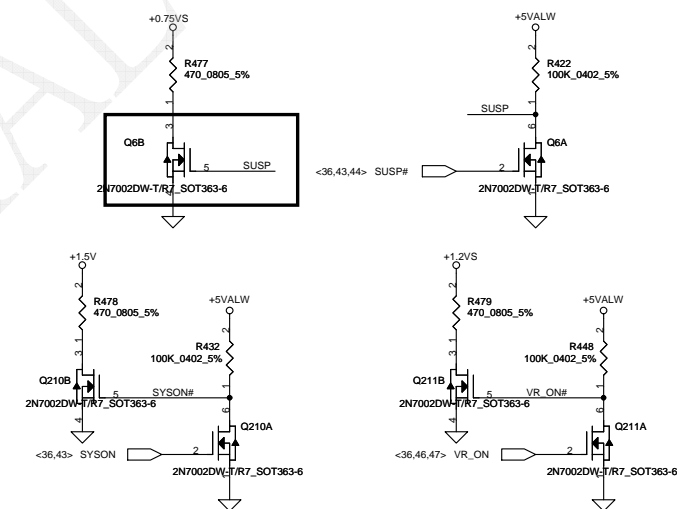
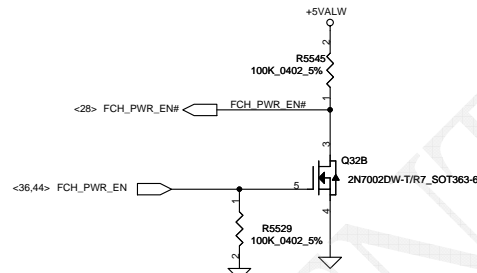
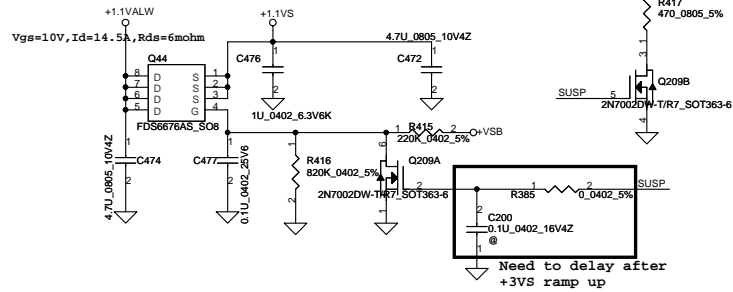
+5VALW TO +5VS



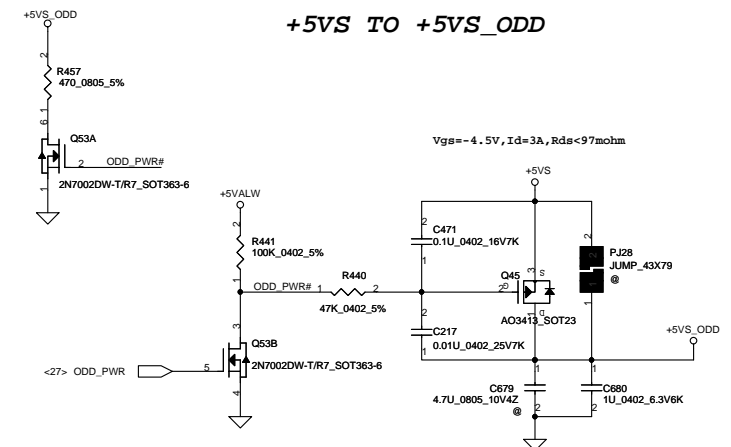
+1.5V to +1.5VS



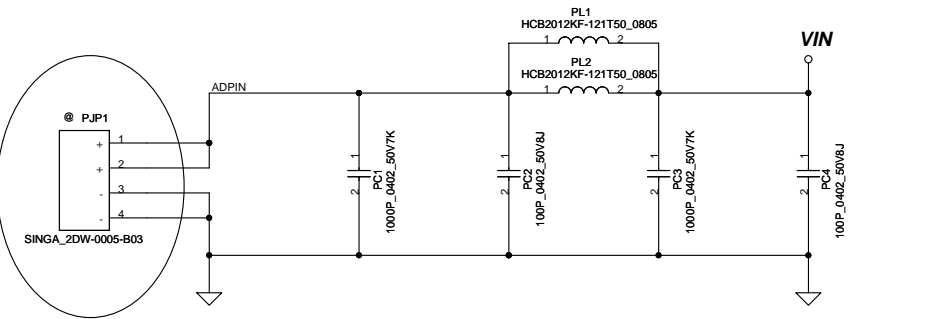
+1.1VALW to +1.1VS



+5VS TO +5VS_ODD

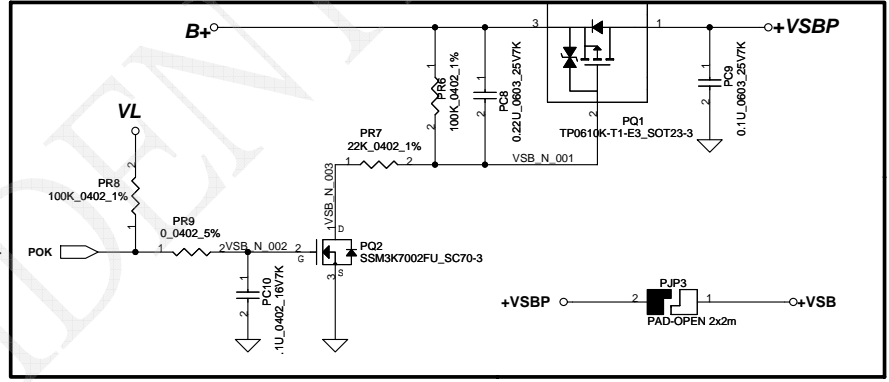
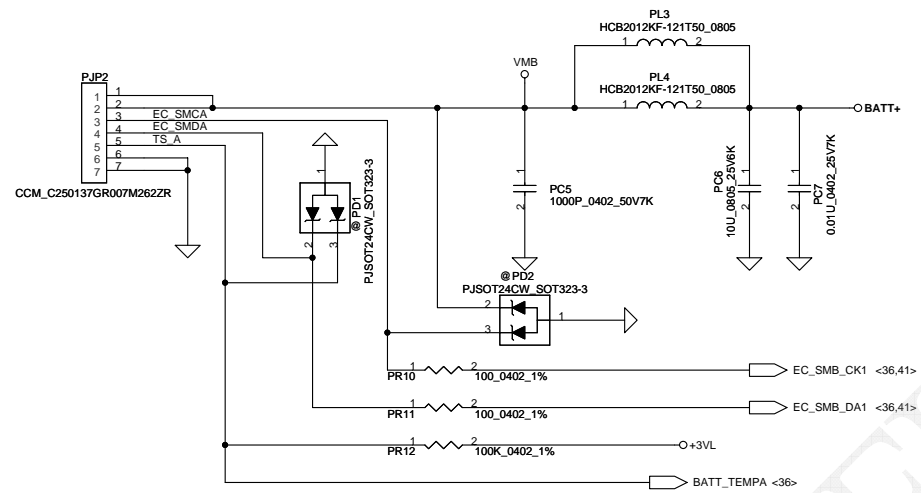
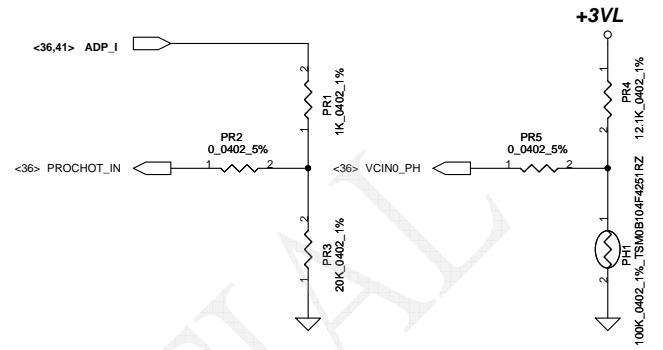


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Date:	Friday, March 23, 2012	Sheet	38	of	51

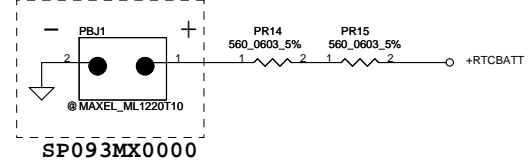


PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

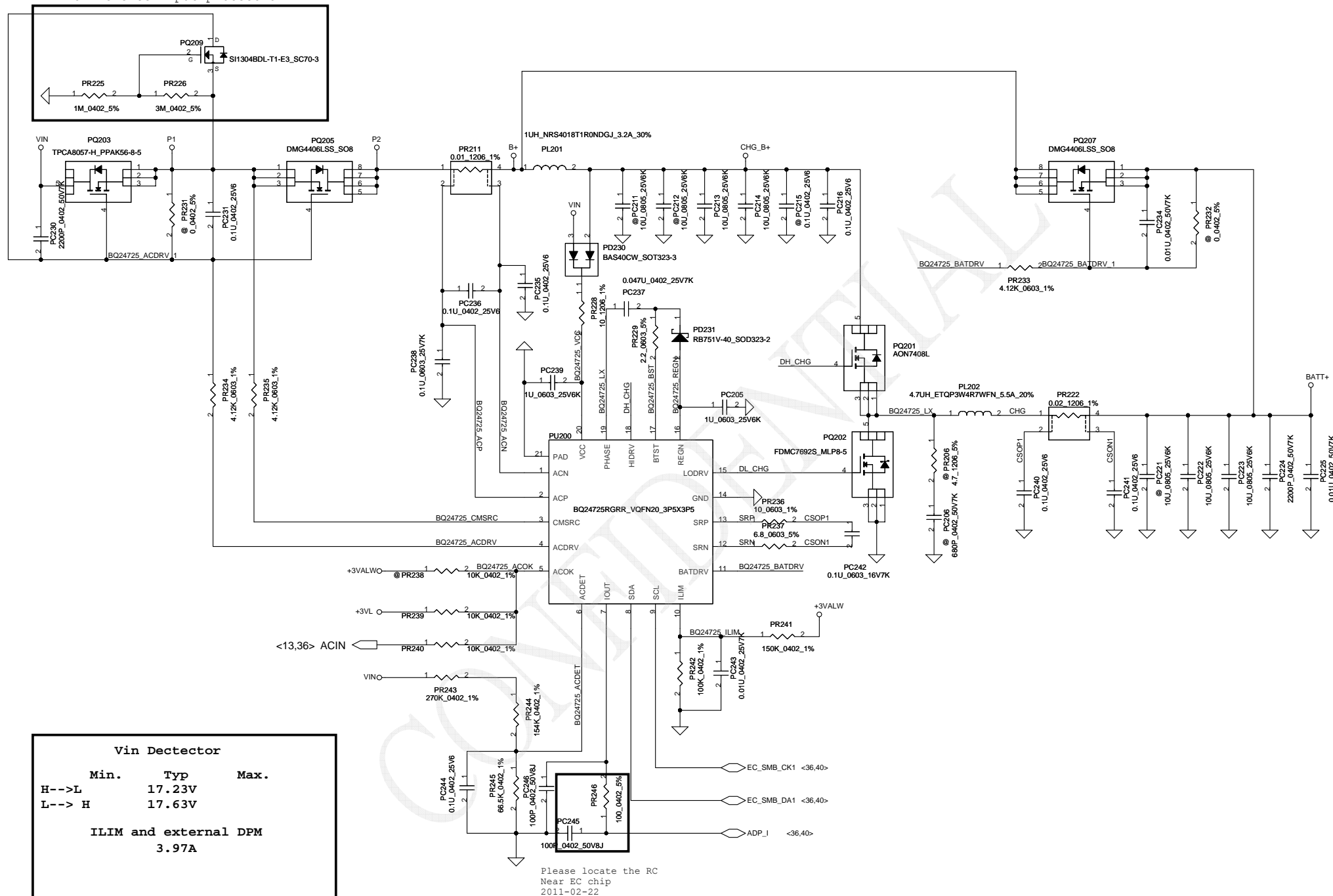
Please locate these parts
Near EC chip

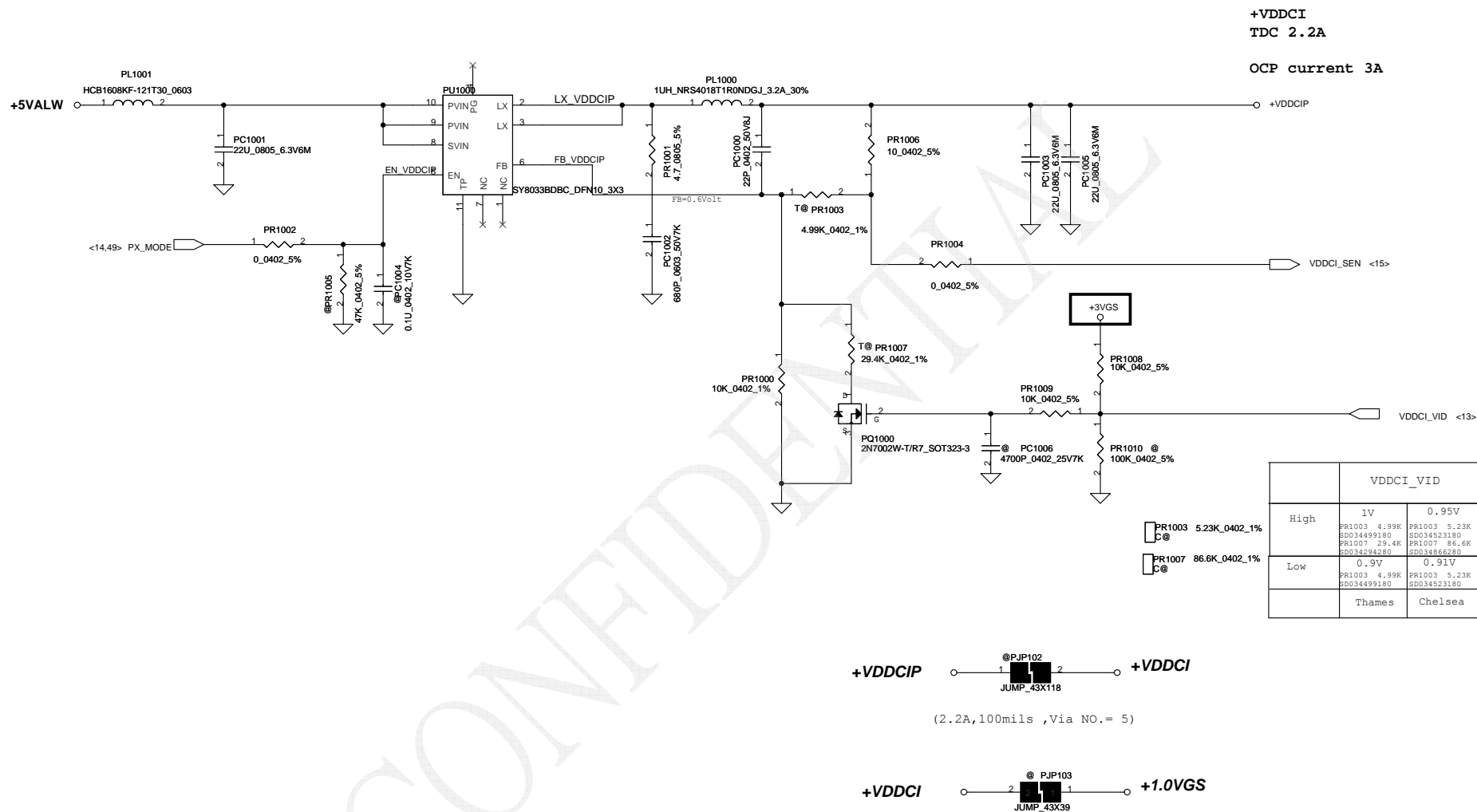


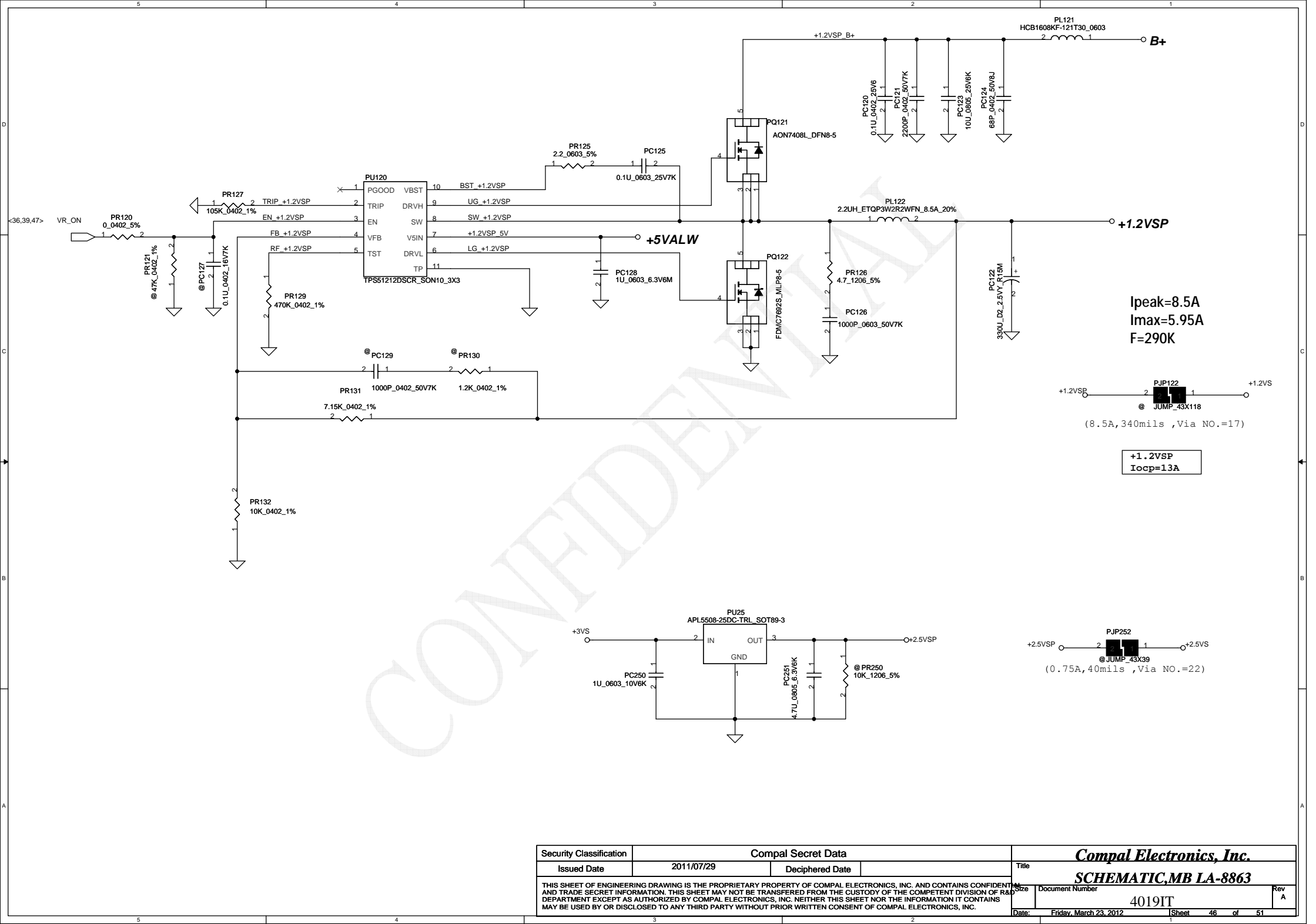
RTC Battery



for reverse input protection







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The schematic diagram illustrates the power supply section of the PCB layout. It features a multi-stage voltage divider network. The input is +VDDC1, which is connected to a series of capacitors (PC973, PC972, PC967, PC936, PC956, PC969, PC954, PC935, PC939, PC934) and resistors (10u, 0402, 6.3V6K) to a central node. This central node is connected to a series of capacitors (PC921, PC922, PC930) and resistors (10u, 0603, 6.3V6M) leading to the output. The output is labeled +VDDC1.

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HW PIR (Product Improve Record)

QMLE4 LA-8863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2012/02/10

Item	Date	Page	Solution	Request
1.	1/10	P32	Add PJ31	For saving power consumption
2.	1/12	P38	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P35	Add internal MIC to MB	For customer request
4.	2/2	P14	Remove PX4.0 circuit	Support PX5.0
5.	2/2	P31	Add PJ26,PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P33	Update JCRI0 pin definition	Change int. MIC to MB
7.	2/2	P35	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P31	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P31	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/7	P32	Change UL3 and UL4 PN to SP050005V00	For shortage

REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P24	Add C201 and C214	For EMI request
9.	3/12	P30	Add C364 and C365	For EMI request
10.	3/12	P35	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/02/14	P40-PWR-DCIN/BATT CONN/OTP	Delete PR12,PR13	Circuit modify
2.	2012/02/14	P41-PWR-CHARGER	Change PR211 to 0.01_1206_1%,PL201 to1UH 4*4*2 Add PC207,PC208,PC217,PC2I8,Delete PC232,PC233	Circuit modify
3.	2012/02/14	P43-PWR-1.5VP/+0.75VSP	Change PL152 to SH00000KS00	Circuit modify
4.	2012/02/14	P44-PWR-+1.1VALWP/+1.8VSP	Change PR718 to 47K,add PC187	HW request
5.	2012/02/14	P46-+1.2VSP/+2.5VSP PR127 to SD034105380	Change PL122 to 2.2uH(SH00000MR00),	Circuit modify
6.	2012/02/14	P37-PWR +CPU CORE	Change PQ502 to TPCA8057	Circuit modify
7.	2012/03/06	P40-PWR-DCIN/BATT CONN/OTP	Add PR12(100KQ)	Circuit modify

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Date: Friday, March 23, 2012				Sheet	51 of 51